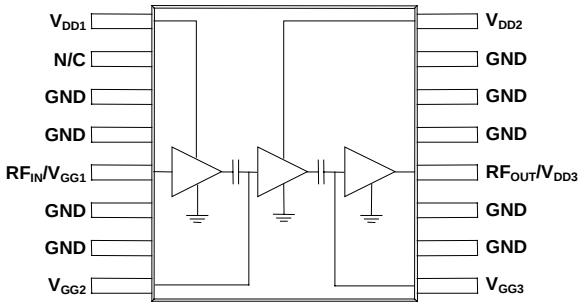
3.6V 0.5W RF Power Amplifier IC for DECT

Applications

DECT
PCS
Personal Wireless Telephony (PWT)
Cordless PBX
Radio/Wireless Local Loop (RLL/WLL)

Features

- Single Positive Supply
- 54% Power Added Efficiency
- 100% Duty Cycle
- 1.2:1 Input VSWR in both On and Off states
- 1800 to 2000 MHz Operation
- 16 Pin TSSOP Plastic Package
- Accommodates Battery Charging Conditions up to 5.5 Volts
- Self-Aligned MSAG®-Lite MESFET Process



54% PAE
100% Duty Cycle

ELECTRICAL CHARACTERISTICS

V_{DD}= 3.6 V, P_{IN}= -2 dBm, T_A=25 °C, Output externally matched to 50 Ω

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	f	1880		1930	MHz
Output Power, f = 1900 MHz	P_{OUT}	26.2	27.2	28.2	dBm
Power Gain	G_P		29.3		dB
Gain Slope, f=1930 to 1880 MHz	—		0.008	0.012	dB/MHz
Power Added Efficiency, f = 1900 MHz	η	49	54		%
Drain Current	I_{DD}		270		mA
Harmonics	$2f_o$ $3f_o$		-34 -38	-30 -34	dBc dBc
Input VSWR (V_{DD} = 0.0 V) (V_{DD} = 3.6 V)	— —		1.2:1 1.2:1	2.0:1 2.0:1	— —
Off Isolation (V_{DD}=0 V)	—	40			dB
Thermal Resistance (Junction of 3rd stage FET to solder point of pin 13)	$R_{TH\ J\text{-}S}$			51	°C/W
Load Mismatch (V_{DD} = 5.5 V, VSWR = 8:1, P_{IN} = -2 dBm)	—	No Degradation in Power Output			
Stability (P_{IN} = -2 dBm, V_{DD} = 0-5.5 V, T_S= -40 to +85 °C, Load VSWR = 5:1)	—	All non-harmonically related outputs more than 60 dB below desired signal			

Specifications subject to change without notice.

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 1, 12, 16)	V_{DD}	5.5	Vdc
RF Input Power	P_{IN}	3	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-40 to +150	°C

APP LICATION INFORMATION

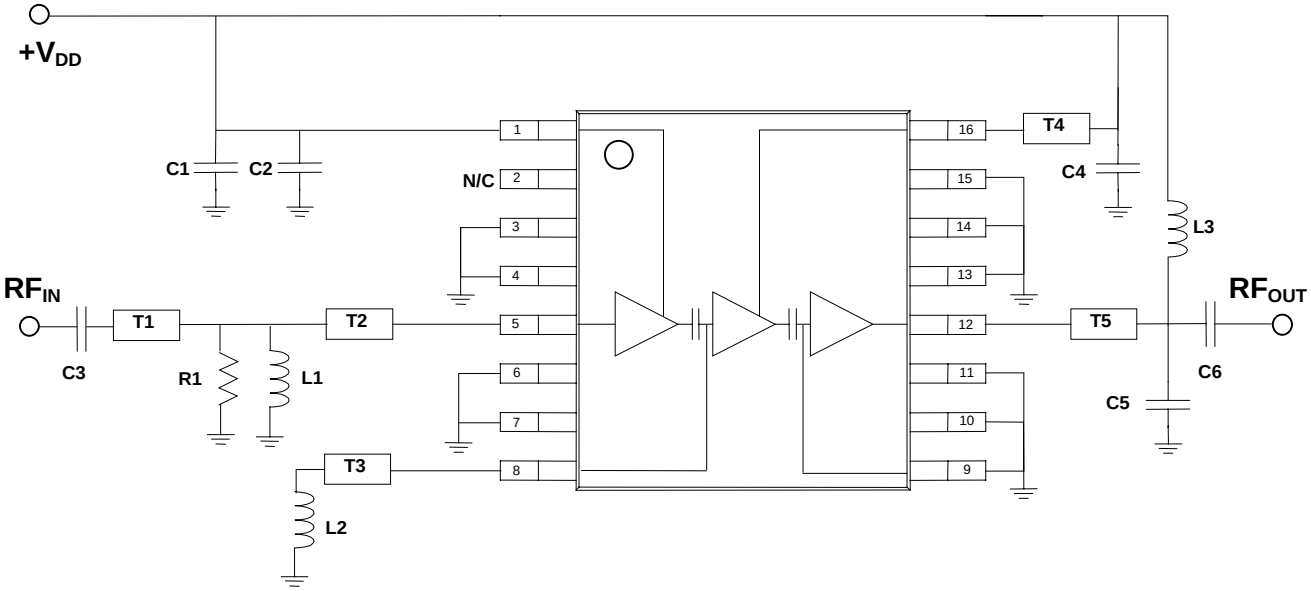


Figure 1. Evaluation Board Schematic

List of components:
C1 = 100 pF DLI multilayer ceramic chip capacitor (C11AH101K5TXL)
C2 = 10 pF DLI multilayer ceramic chip capacitor (C11AH1R0B5TXL)
C3 = 0.7 pF DLI multilayer ceramic chip capacitor (C11AH0R7B5TXL)
C4 = 10 pF DLI multilayer ceramic chip capacitor (C11AH1R0B5TXL)
C5 = 2.2 pF DLI multilayer ceramic chip capacitor (C11AH2R2B5TXL)
C6 = 100 pF DLI multilayer ceramic chip capacitor (C11AH101K5TXL) (DC blocking capacitor)
L1 = 2.7 nH Toko chip inductor (TKS2362CTND)
L2 = 3.3 nH Toko chip inductor (TKS2363CTND)
L3 = 27 nH Coilcraft chip inductor (1008CS.270XMBB)
R1 = 300 Ω chip resistor

T1 = 0.19" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)
T2 = 0.12" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)
T3 = 0.39" of 75 Ω grounded coplanar waveguide (60 mil GETEK board)
T4 = 0.11" of 75 Ω grounded coplanar waveguide (60 mil GETEK board)
T5 = 0.14" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)

Component layout and printed circuit board drawing for RF IC evaluation board are shown in Figure 9.

TYPICAL CHARACTERISTICS

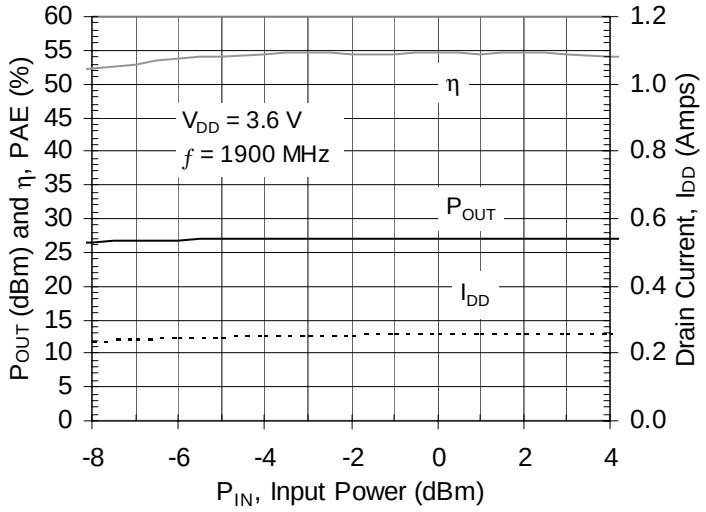


Figure 2. Output power, drain current and efficiency vs. input power

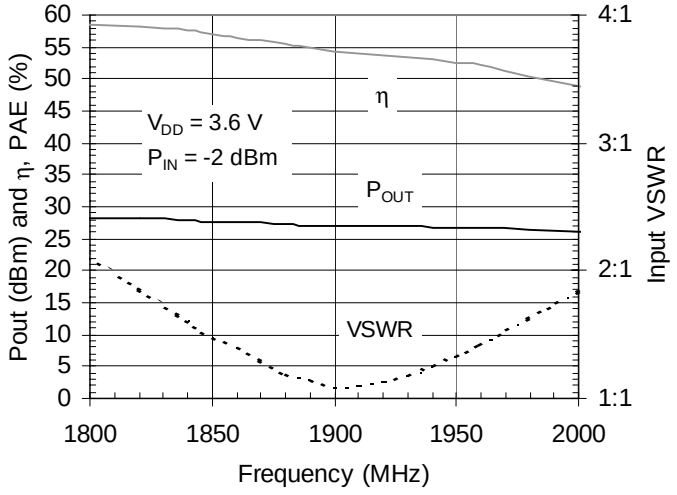


Figure 3. Output power, efficiency and input VSWR vs. frequency

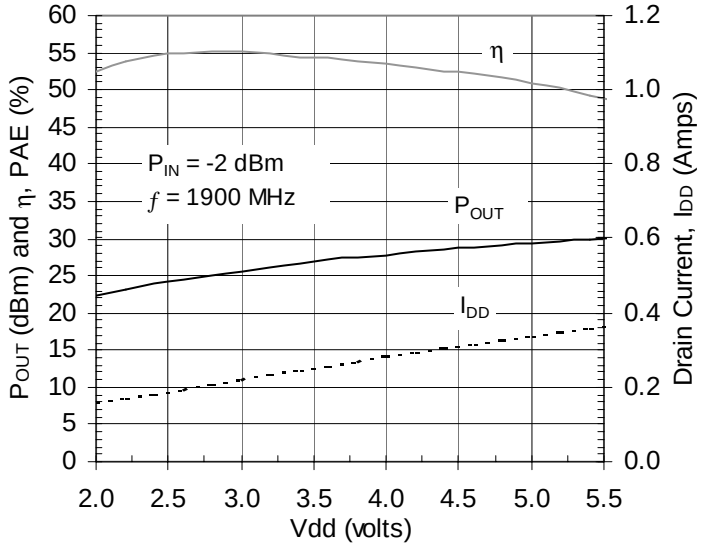


Figure 4. Output power, drain current and efficiency vs. supply voltage

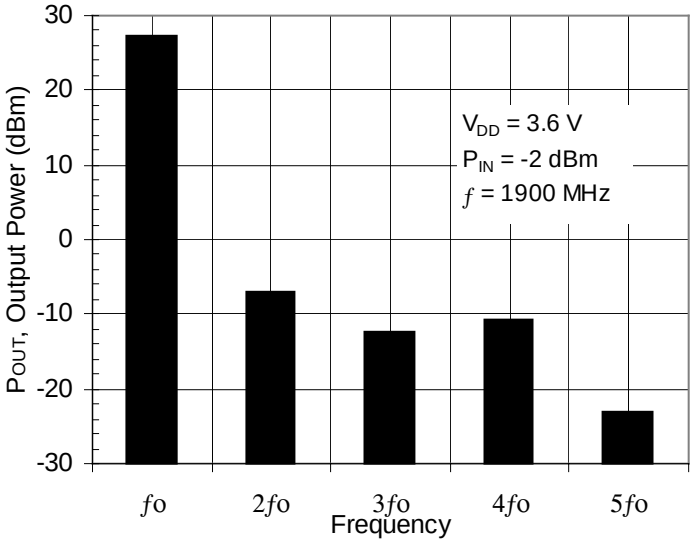


Figure 5. Harmonics

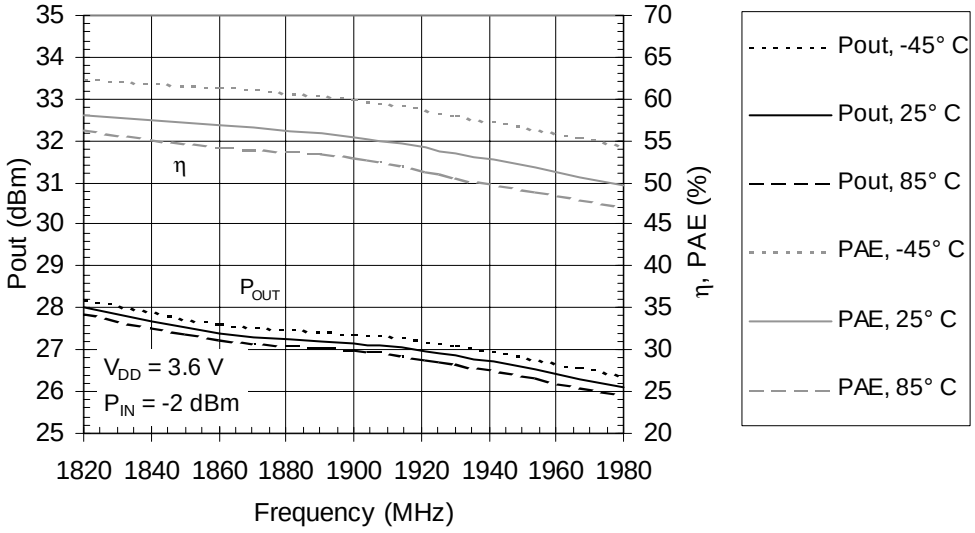


Figure 6. Output power and efficiency vs. frequency for different ambient temperatures

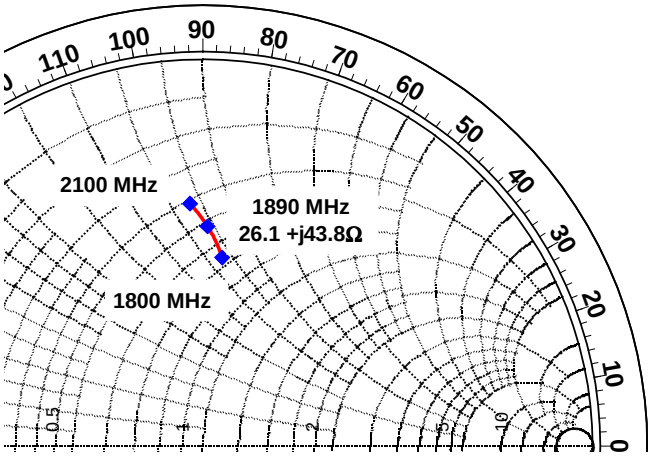


Figure 7. Input match impedance (as seen from the end of pin 5 without IC on board)

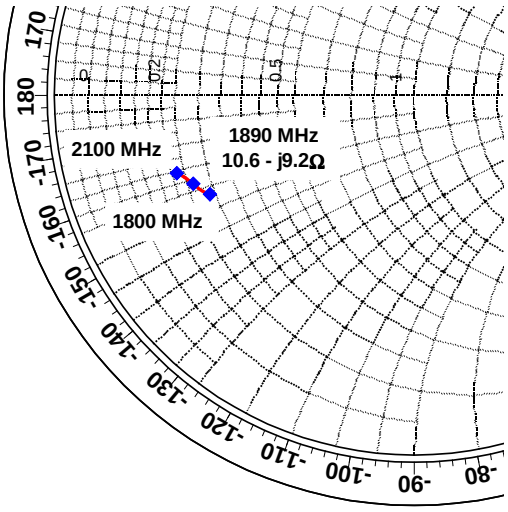


Figure 8. Output match impedance (as seen from the end of pin 12 without IC on board)

Specifications subject to change without notice.

MECHANICAL DATA

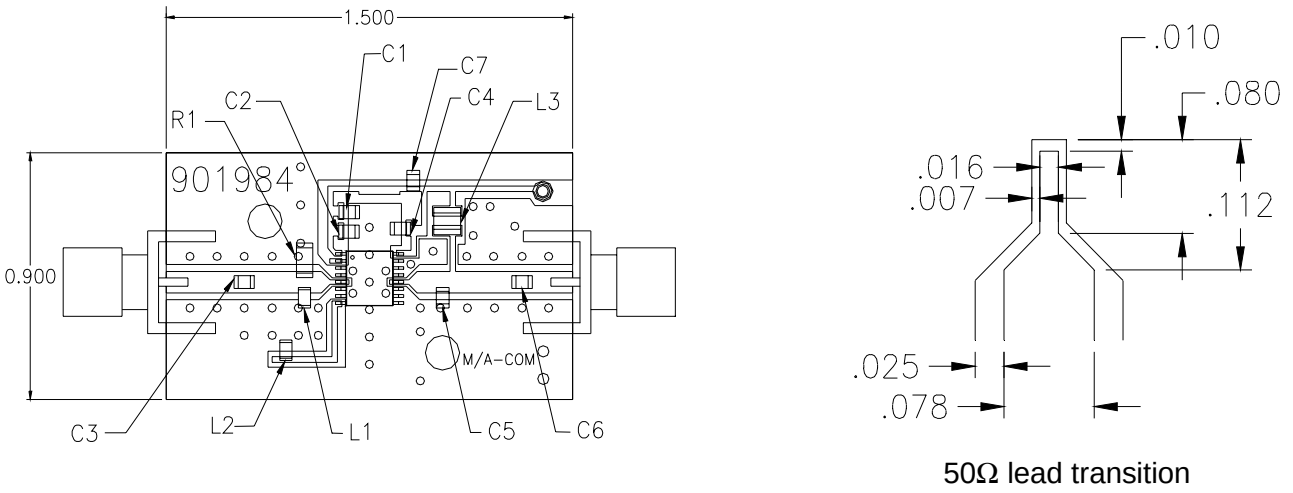


Figure 9. Component layout and printed circuit drawing for evaluation board (units in inches)