MAY 1997
Revision 1.1

LXT970

Fast Ethernet Transceiver

General Description

The LXT970 Fast Ethernet Transceiver supports IEEE 802.3 compliant Ethernet applications at both 10 and 100Mbps operation. It provides the active circuitry to interface 802.3 media independent interface (MII) compliant controllers to 10BASE-T and/or 100BASE-TX media. The LXT970 also provides an ECL-type interface for use with 100BASE-FX fiber networks.

The LXT970 supports full duplex operation at 10 and 100 Mbps. Its operating condition can be set using auto-negotiation, parallel detection or manual control. The encoder can be bypassed for symbol mode applications.

The LXT970 is fabricated with an advanced CMOS process and requires only a single 5 volt power supply. The MII may be operated independently with either a 5 volt supply or a 3.3 volt supply.

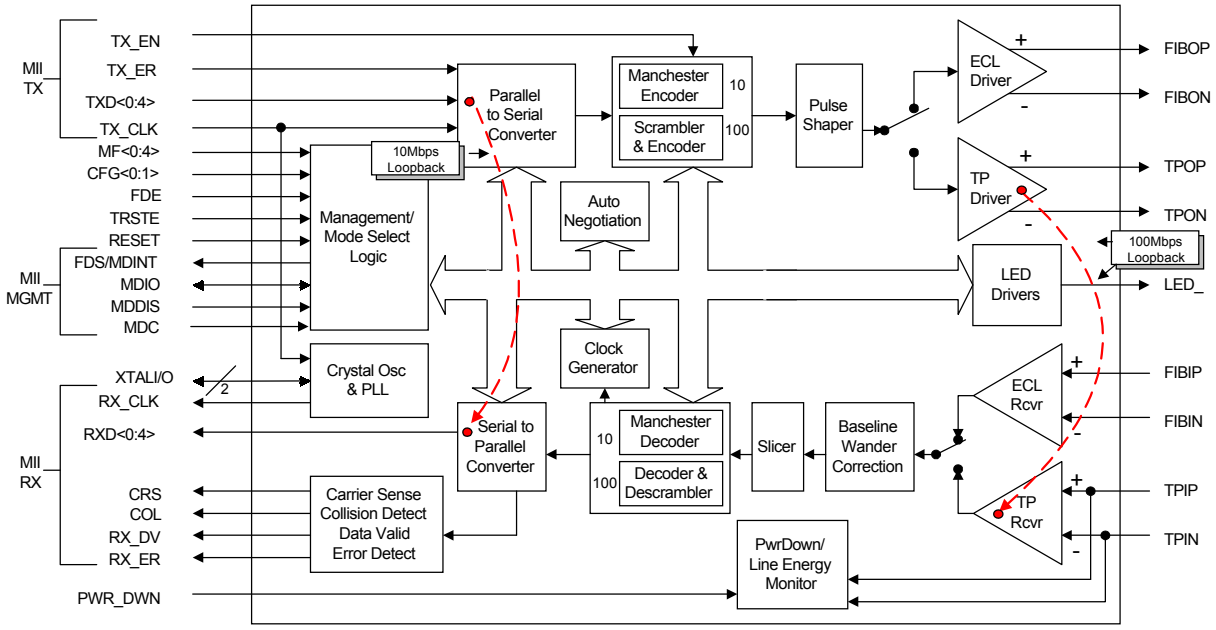
Applications

- Combination 10BASE-T/100BASE-TX Network Interface Cards (NICs)
- 10/100 Switches, 10/100 Repeaters
- 100BASE-FX Network Interface Cards (NICs)

Features

- IEEE 802.3 Compliant:
  - 10BASE-T and 100BASE-TX using a single RJ45 connection
  - Supports both auto-negotiation via Fast Link Pulse (FLP) exchange and parallel detection for legacy 10BASE-T and 100BASE-TX systems
  - MII interface with extended register capability
- Baseline wander correction
- 100BASE-FX fiber optic capable
- Standard CSMA/CD or full duplex operation at 10 or 100 Mbps
- Configurable through MII serial port or via external control pins
- Configurable for DTE, repeater or switch applications
- CMOS process with single 5 volt supply operation with provision for interface to 3.3 V MII bus
- Integrated transmit and receive filtering for 10BASE-T and 100BASE-TX
- Integrated LED drivers
- Integrated supply monitor and line disconnect during low supply fault

LXT970 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT970 Pin Assignments and Signal Descriptions

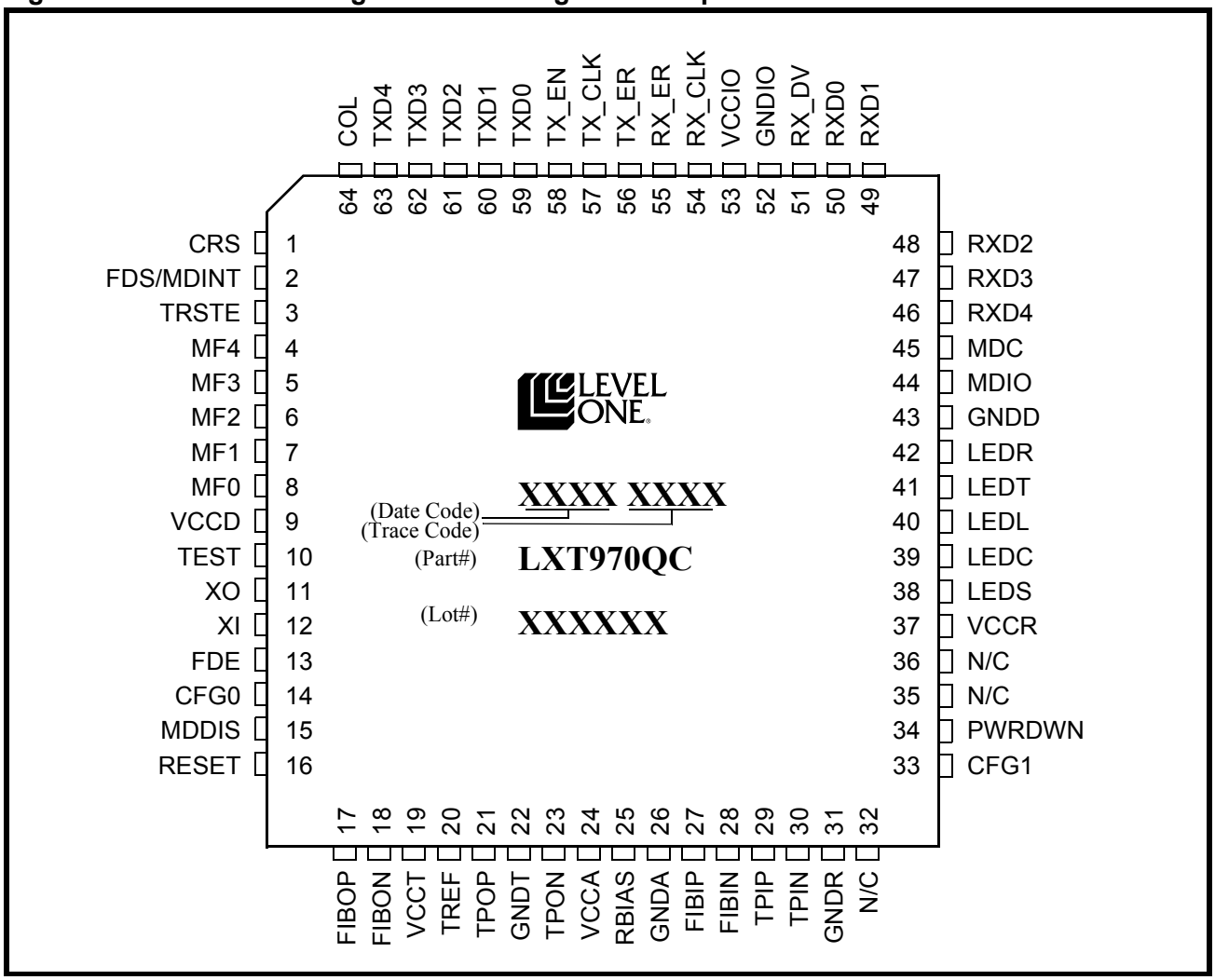


Table 1: LXT970 Power Supply Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
19 22	VCCT GNDT	-	**Transmitter Supply** (+5V) and **Ground**.
37 31	VCCR GNDR	-	**Receiver Supply** (+5V) and **Ground**.
24 26	VCCA GNDA	-	**Analog Supply** (+5V) and **Ground**.
9 43	VCCD GNDD	-	**Digital Supply** (+5V) and **Ground**.
53 52	VCCIO GNDIO	-	**MII Supply** (+3.3V or +5V) and **Ground**.

Table 2: LXT970 MII Signal Descriptions

Pin#	Pin Name	I/O[1]	Pin Description
			MII Data Interface Pins
63 62 61 60 59	TXD4 TXD3 TXD2 TXD1 TXD0	I	**Transmit Data**. The MAC drives data to the LXT970 using these inputs. TXD4 is monitored only in Symbol (5B) Mode. These signals must be synchronized to the TX_CLK.
58	TX_EN	I	**Transmit Enable**. The MAC asserts this signal when it drives valid data on the TXD inputs. This signal must be synchronized to the TX_CLK.
57	TX_CLK	I/O	**Transmit Clock**. 25 MHz for 100 Mbps operation, 2.5 MHz for 10 Mbps operation. Refer to the Clock Requirements discussion in the Functional Description section.
56	TX_ER	I	**Transmit Coding Error**. The Media Access Controller (MAC) asserts this input when an error has occurred in the transmit data stream. When the LXT970 is operating at 100Mbps, the LXT970 responds by sending "Invalid Code Symbols" on the line.
46 47 48 49 50	RXD4 RXD3 RXD2 RXD1 RXD0	O	**Receive Data**. The LXT970 drives received data on these outputs, synchronous to RX_CLK. RXD4 is driven only in Symbol (5B) Mode.
51	RX_DV	O	**Receive Data Valid**. The LXT970 asserts this signal when it drives valid data on RXD. This output is synchronous to RX_CLK.
55	RX_ER	O	**Receive Error**. The LXT970 asserts this output when it receives invalid symbols from the network. This signal is synchronous to RX_CLK.
54	RX_CLK	O	**Receive Clock**. 25 MHz for 100 Mbps operation, 2.5 MHz for 10 Mbps operation. Refer to the Clock Requirements discussion in the Functional Description section.
64	COL	O	**Collision Detected**. The LXT970 asserts this output when a collision is detected. This output remains High for the duration of the collision. This signal is asynchronous and is inactive during full duplex operation.
1	CRS	O	**Carrier Sense**. During half-duplex operation (bit 0.8 = 0)[2], the LXT970 asserts this output when either transmit or receive medium is non-idle. During full-duplex operation (bit 0.8 = 1) or repeater operation (bit 19.13 = 1), CRS is asserted only when the receive medium is non-idle.
3	TRSTE	I	**Tristate**. In DTE Mode (19.13 = 0), when TRSTE input is High, the LXT970 isolates itself from the MII Data Interface, and controls the MDIO register bit 0.10 (Isolate bit). When MDDIS is High, TRSTE provides continuous control over bit 0.10. When MDDIS is Low, TRSTE sets initial (default) values only and reverts control back to the MDIO interface. In Repeater Mode (19.13 = 1), when TRSTE input is High, the LXT970 tri-states the receive outputs of the MII (RXD<4:0>, RX_DV, RX_ER, RX_CLK).

1. I/O Column Coding: I = Input, O = Output, OD = Open Drain
2. The LXT970 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-31) and Y is the bit number (0-15).

Table 2: LXT970 MII Signal Descriptions – continued

Pin#	Pin Name	I/O[1]	Pin Description
			MII Control Interface Pins
15	MDDIS	I	**Management Disable**. When MDDIS is High, the MDIO is restricted to Read Only and the MF<4:0>, CFG<1:0> and FDE pins provide continual control of their respective bits. When MDDIS is Low at power up or Reset, the MF<4:0>, CFG<1:0> and FDE pins control only the initial or "default" values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
45	MDC	I	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 2.5 MHz.
44	MDIO	I/O	**Management Data Input/Output**. Bidirectional serial data channel for PHY/STA communication.
2	FDS/MDINT	OD	**Full Duplex Status**. When bit 17.1 = 0 (default), this pin indicates full duplex status. (High = Full Duplex, Low = Half Duplex) This pin can drive a high efficiency LED. (See Table 22 for detail specifications). **Management Data Interrupt**. When bit 17.1 = 1, an active Low output on this pin indicates status change. Interrupt is cleared by sequentially reading Register 1, then Register 18.

1. I/O Column Coding: I = Input, O = Output, OD = Open Drain
2. The LXT970 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-31) and Y is the bit number (0-15).

Table 3: LXT970 Fiber Interface Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
17 18	FIBOP FIBON	O	**Fiber Output, Positive and Negative**. Differential pseudo-ECL driver pair compatible with standard fiber transceiver for 100BASE-FX.
27 28	FIBIP FIBIN	I	**Fiber Input, Positive and Negative**. Differential pseudo-ECL receive pair compatible with standard fiber transceiver for 100BASE-FX.

1. I/O Column Coding: I = Input, O = Output

Table 4: LXT970 Twisted Pair Interface Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
21 23	TPOP TPON	AO	**Twisted Pair Output, Positive and Negative**. Differential driver pair produces 802.3-compliant pulses for either 100BASE-TX or 10BASE-T transmission.
20	TREF	AO	**Transmit Reference**. Tie to center tap of output transformer.
29 30	TPIP TPIN	AI	**Twisted Pair Input, Positive and Negative**. Differential input pair for either 100BASE-TX or 10BASE-T reception.

1. I/O Column Coding: I = Input, O = Output, A = Analog

Table 5: LXT970 LED Indicator Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
38	LEDS	O	**Speed LED**. Active Low output indicates 100 Mbps operation is selected.
42	LEDR	O	**Receive LED**. Active Low output indicates that receiver is active.
41	LEDT	O	**Transmit LED**. Active Low output indicates transmitter is active.
40	LEDL	O	**Link LED**. Active Low output; During 100 Mbps operation, indicates scrambler lock and receipt of valid Idle codes. During 10 Mbps operation, indicates Link Valid status.
39	LEDC	O	**Collision LED**. In default mode, active Low output indicates collision. However, LEDC is programmable and may be set for other indications. For programming options, see Configuration Register 19 in Table 53.

1. I/O Column Coding: O = Output

Table 6: LXT970 Miscellaneous Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
10	TEST	I	**Test**. Must be tied Low.
12 11	XI XO	I O	**Crystal Input and Output**. A 25 MHz crystal oscillator circuit can be connected across XI and XO. A clock can also be used at XI. Refer to Functional Description for detailed clock requirements.
25	RBIAS	AI	**Bias Control**. Controls operating circuit bias via an external 22 kΩ, 1% resistor to ground.
16	RESET	I	**Reset**. This active Low input is OR'ed with the control register Reset bit (0.15). The LXT970 reset cycle is extended 205ns (nominal) after Reset is de-asserted.
34	PWRDWN	I	**Power Down**. When High, forces LXT970 into power down mode. This pin is OR'ed with the Power Down bit (0.11). Refer to Table 43 for more information.
32, 35, 36	N/C	-	**No Connection**. Leave open.

1. I/O Column Coding: I = Input, O = Output, A = Analog

Table 7: LXT970 Hardware Control Interface Signal Descriptions

Pin#	Pin Name	I/O	Pin Description
	MF0 - MF4	I	**Multi-Function (MF)**. Each pin has two independent settings that are established by 4-level supply voltages. The first setting (ADD), determines the PHY address on the MDIO bus and the second setting (FUNC), determines configuration of the LXT970. The MF inputs directly affect particular bits in the MDIO register set. The effect is mediated by the MDDIS pin. When MDDIS is High, these inputs continually affect the MDIO registers. When MDDIS is Low, they determine initial (default) values only. Table 21 shows the 4-level supply voltages (voltage levels referred to as VMF1, VMF2, VMF3 and VMF4) that establish the settings per pin. An external voltage divider, as shown in the Layout Requirement section, is required to establish mid-level (VMF2 and VMF3) settings. VMF1 and VMF4 (default) settings, can be established with the LXT970 standard power supply and do not require a voltage divider. Tables 8 and 9 show the selected MF pin function and address with respect to the applied input voltage level. The descriptions below detail the configuration of each of these pins.
8	MF0	I	Enables Auto-Negotiation (A/N) and directly affects MDIO register bit 0.12. When input value = VMF1 or VMF4, A/N is disabled and 0.12 = 0. When input value = VMF2 or VMF3, A/N is enabled and 0.12 = 1.
7	MF1	I	Selects Repeater Mode and directly affects MDIO register bit 19.13. When input value = VMF1 or VMF4, DTE Mode is enabled and 19.13 = 0. When input value = VMF2 or VMF3, Repeater Mode is enabled and 19.13 = 1.
6	MF2	I	In TX mode, selects 4B Nibble (normal) or 5B Symbol Mode and directly affects MDIO register bit 19.4. When input value = VMF1 or VMF4, 4B Nibble Mode is selected and 19.4 = 0. When input value = VMF2 or VMF3, 5B Symbol Mode is selected and 19.4 = 1.
5	MF3	I	In TX mode, enables or bypasses Scrambler operation and directly affects MDIO register bit 19.3. When input value = VMF1 or VMF4, Scrambler is enabled and 19.3 = 0. When input value = VMF2 or VMF3, Scrambler is bypassed and 19.3 = 1. In FX mode, the LXT970 *automatically* bypasses the Scrambler. *Selecting* Scrambler bypass in FX mode will cause the LXT970 to also bypass the 4B/5B encoder and enable Symbol mode MII operation.
4	MF4	I	**When A/N is enabled**, MF4 determines operating speed advertisement capabilities in combination with CFG1. See Table 9 for details. **When A/N is disabled**, this input selects either TX or FX interface. When FX interface is selected, the LXT970 will automatically disable the scrambler. For correct FX operation, 100Mbps operation must also be selected. When input value = VMF1 or VMF4, TX is enabled and 19.2 = 0. When input value = VMF2 or VMF3, FX is enabled and 19.2 = 1.

1. I/O Column Coding: I = Input

Table 7: LXT970 Hardware Control Interface Signal Descriptions – continued

Pin#	Pin Name	I/O	Pin Description
13	FDE	I	**Full Duplex Enable**. **When A/N is enabled**, FDE determines full duplex advertisement capability in combination with MF4 and CFG1. See Table 9 for details. **When A/N is disabled**, FDE directly affects full duplex operation and determines the value of bit 0.8 (Duplex Mode). When FDE is High, F/D is enabled and 0.8 = 1. When FDE is Low, F/D is disabled and 0.8 = 0.
14	CFG0	I	**Configuration Control 0**. **When A/N is enabled,** Low to High transition on CFG0 causes auto-negotiate to re-start and 0.9 = 1. **When A/N is disabled**, this input selects operating speed and directly affects bit 0.13. When CFG0 is High, 100Mbps is selected and 0.13 = 1. When CFG0 is Low, 10Mbps is selected and 0.13 = 0.
33	CFG1	I	**Configuration Control 1**. **When A/N is enabled**, CFG1 determines operating speed advertisement capabilities in combination with MF4. See Table 9 for details. **When A/N is disabled**,CFG1 enables 10Mbps link test function and directly affects bit 19.8. When CFG1 is High, 10Mbps link test is disabled and 19.8 = 1. When CFG1 is Low, 10Mbps link test is enabled and 19.8 = 0.

1. I/O Column Coding: I = Input

Table 8: MF Pin Function Descriptions[1, 3]

Pin	Address	Input Voltage Levels[2]			
	Function	V_{MF1}	V_{MF2}	V_{MF3}	V_{MF4}
MF0	**Address Bit 0**	1	1	0	0
	Auto-Negotiation **Sets the initial value of bit 0.12**	Disabled (0.12 = 0)	Enabled (0.12 = 1)	Enabled (0.12 = 1)	Disabled (0.12 = 0)
MF1	**Address Bit 1**	1	1	0	0
	Repeater / DTE Mode **Sets the initial value of bit 19.13**	DTE (19.13 = 0)	Repeater (19.13 = 1)	Repeater (19.13 = 1)	DTE (19.13 = 0)
MF2	**Address Bit 2**	1	1	0	0
	Nibble (4B) / Symbol (5B) Mode **Sets the initial value of bit 19.4**	Nibble (4B) (19.4 = 0)	Symbol (5B) (19.4 = 1)	Symbol (5B) (19.4 = 1)	Nibble (4B) (19.4 = 0)
MF3	**Address Bit 3**	1	1	0	0
	Scrambler Operation **Sets the initial value of bit 19.3**	Enabled (19.3 = 0)	Bypassed (19.3 = 1)	Bypassed (19.3 = 1)	Enabled (19.3 = 0)
MF4	**Address Bit 4**	1	1	0	0
	If Auto-Negotiate Enabled via MF0, MF4 works in combination with CFG1 to control operating speed and duplex advertisement capabilities via bits 4.5 through 4.8. See Table 9 for details.				
	If Auto-Negotiate Disabled via MF0 Then TX/FX Mode Sets the initial value of bit 19.2	100TX (19.2 = 0)	100FX (19.2 = 1)	100FX (19.2 = 1)	100TX (19.2 = 0)

1. In MDIO Control Mode, the MF pins control only the initial or default value for the respective register bits. In Manual Control mode, the MF pins provide continuous control of the respective register bits.
2. Input Voltage Levels (V_{MF1}, V_{MF2}, V_{MF3}, V_{MF4}) for MF pins.
3. See Tables 10 and 11 for operating configuration set-up.

Table 9: LXT970 Operating Speed/Full Duplex Advertisement Settings

MF4 Input Voltage Levels[2]	CFG1	FDE	MDIO Registers[1]	Function
If Auto-Negotiate Enabled via MF0				
VMF1, VMF4	Low	–	Sets 4.5, 4.6, 4.7 and 4.8 = 1	Advertise all capabilities Ignore FDE
VMF1, VMF4	High	High	Sets 4.5 = 1 Sets 4.7 and 4.8 = 0 Sets 4.6 = 1	Advertise 10 Mbps only FD Advertised
		Low	Sets 4.5 = 1 Sets 4.7 and 4.8 = 0 Sets 4.6 = 0	Advertise 10 Mbps only FD Not Advertised
VMF2, VMF3	Low	High	Sets 4.7 = 1 Sets 4.5 and 4.6 = 0 Sets 4.8 = 1	Advertise 100 Mbps only FD Advertised
		Low	Sets 4.7 = 1 Sets 4.5 and 4.6 = 0 Sets 4.8 = 0	Advertise 100 Mbps only FD Not Advertised
VMF2, VMF3	High	High	Sets 4.5 and 4.7 = 1 Sets 4.6 and 4.8 = 1	Advertise 10/100 Mbps FD Advertised
		Low	Sets 4.5 and 4.7 = 1 Sets 4.6 and 4.8 = 0	Advertise 10/100 Mbps FD Not Advertised

FUNCTIONAL DESCRIPTION

Introduction

The LXT970 Fast Ethernet Transceiver is a physical layer (PHY) device that supports 10 Mbps and 100 Mbps Ethernet networks. It provides all the functions necessary to build an IEEE 802.3 compliant solution. The LXT970 can directly drive a twisted-pair cable for up to 100 meters. The LXT970 also provides a pseudo-ECL interface for driving a 100BASE-FX fiber connection.

On power-up, the LXT970 can use auto-negotiation with parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT970 will auto-negotiate with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT970 will automatically detect the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and set its operating speed accordingly. When the line speed selection is made via the parallel detection method, the duplex mode will be set to half. The user may later select full duplex operation by subsequent writes to the appropriate MDIO register. Line operation can also be set using the Hardware Control Interface.

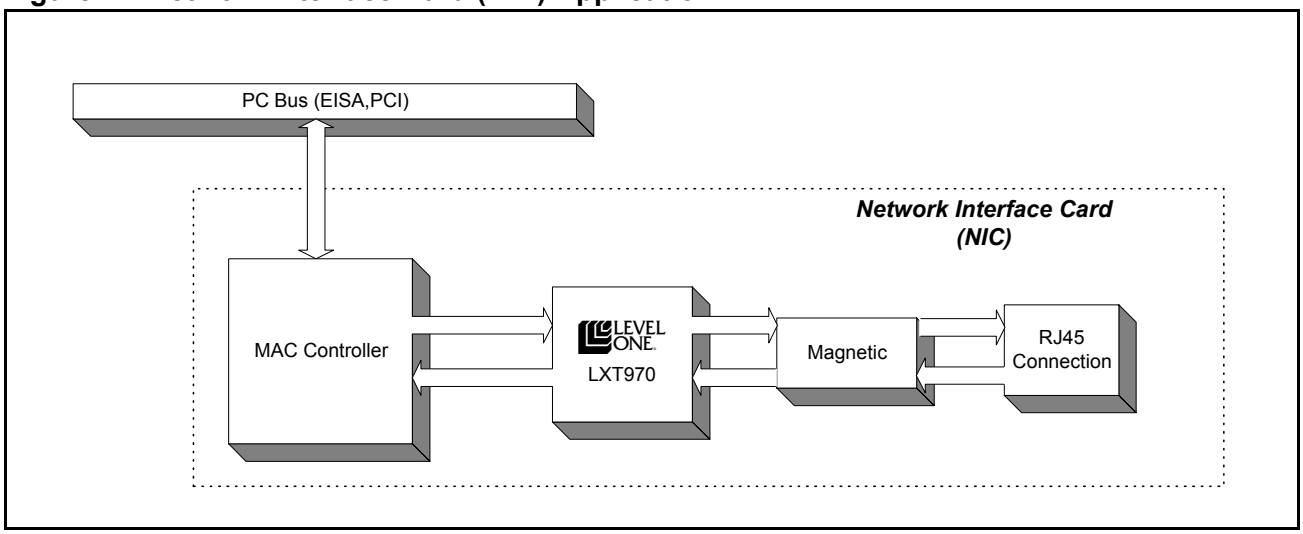
The LXT970 interfaces to a 10/100 MAC through the MII interface. The LXT970 performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X specification. It also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections. The MII speed is automatically set once line operating conditions have been determined.

The LXT970 supports NIC, repeater and switch applications. It provides half- and full-duplex operation at 100Mbps and 10Mbps. See Figure 2 for a typical Network Interface Card (NIC).

NOTE

The LXT970 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register address (0-31) and Y is the bit number (0:15).

Figure 2: Network Interface Card (NIC) Application



Network Media / Protocol Support

The LXT970 supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair, or 100 Mbps Ethernet over fiber media (100BASE-FX). A standard Media Independent Interface (MII) is used for communication with the Media Access Controller (MAC).

10/100 Mbps Twisted Pair Interface

The twisted-pair interface consists of two differential pairs: the Twisted-Pair Input (TPIP/N) for receiving data, and the Twisted-Pair Output (TPOP/N) for transmitting data. This interface is used for both 10Mbps and 100Mbps operation. Auto-negotiation/parallel detection or manual control can be used to determine operation of the twisted-pair interface.

When operating at 100Mbps, MLT3 symbols are continuously transmitted and received. When not transmitting data, the LXT970 generates ”IDLE” symbols.

During 10Mbps operation, Manchester encoded data is exchanged. During idle periods, the line is left in an idle voltage state.

In 100Mbps mode, the LXT970 is capable of driving a 100BASE-TX connection over 100Ω, Category 5, Unshielded Twisted Pair (UTP). A 10BASE-T connection can be supported using 100Ω, Category 3 or Category 5, UTP.

A transformer with 1:1 windings for transmit and receive, load resistors and bypass capacitors are all that is needed to complete this interface. The Transmit Reference (TREF) pin is used to supply +5V to the output transformer center tap. Using Level One's patented waveshaping technology, the transmitter pre-distorts the outgoing signal to reduce the need for external filters for EMI compliance.

When the twisted-pair interface is selected the FIBOP/N drivers are disabled. All data presented on the FIBIP/N input pins is ignored. In applications where the fiber interface is not used, the fiber I/O pins (FIBIP/N and FIBOP/N) may be left unconnected.

100 Mbps Fiber Interface

The LXT970 provides a pseudo-ECL interface that complies with the ANSI X3.166 specification. This interface is suitable for driving a fiber-optic coupler. This interface consists of four signals: FIBIP/N are the input pair and FIBOP/N are the output pair. The Fiber Port cannot be enabled via auto-negotiation, it must be enabled via the Hardware Control Interface or MDIO registers. When the fiber interface is selected, the TPOP/N drivers are disabled and the TREF pin is tri-stated. All data presented on the TPIP/N input pins is ignored. In applications where the twisted pair interface is not used, the twisted pair I/O pins (TPIP/N, TPOP/N and TREF) may be left unconnected.

MII Interface

The MII Interface is specified in IEEE 802.3. For this discussion, the MII is divided into two blocks; the MII Data Interface and the MII Management Interface.

MII Data Interface

This interface is used to pass data between the LXT970 and a Media Access Controller (MAC). The MII operates at either 2.5 MHz or 25 MHz, depending on the network link speed.

Ten signals are used to pass received data to the MAC: RXD<4:0>, RX_CLK, RX_DV, RX_ER, COL and CRS. Eight signals are used to transmit data from the MAC: TXD<4:0>, TX_CLK, TX_EN, and TX_ER.

Nibble (4B) vs. Symbol (5B) Mode

In nibble mode (19.4 = 0), 4-bit nibbles are passed across the MII data interface. RXD4 is set Low and TXD4 is ignored.

In symbol mode (19.4 = 1), 5-bit symbols are passed across the MII data interface. RXD4 and TXD4 are active.

DTE vs. Repeater Mode

In DTE mode (19.13 = 0), the LXT970 asserts RX_DV, RXD, RX_CLK and RX_ER as soon as it receives a packet from the network. In repeater mode (19.13 = 1), when TRSTE input is High, these output signals are tri-stated. This allows multiple LXT970’s to share a single MII Interface and an external arbiter to determine which LXT970 should drive the MII Data Interface.

Loopback Operation

Loopback is determined by the operational state of the device and by bits 0.14 and 19.11. Bit 0.14 controls MII loopback test at both 10 and 100Mbps. Bit 19.11 controls normal twisted-pair loopback during 10Mbps, half-duplex operation. CRS is generated when the LXT970 is receiving data during all modes of operation.

- Full Duplex - During full duplex mode loopback and collision detection are always disabled. CRS is not generated on transmission.

- Repeater Mode - (bit 19.13 = 1) During repeater mode, loopback is disabled. CRS is not generated on transmit and collision detection is enabled.
- Half-Duplex/DTE Mode (10Mbps) - If 19.11 = 0 (default), data is looped back. If 19.11 = 1, data is not looped back. In both cases CRS is generated on transmit and collision detection is enabled.
- Half-Duplex/DTE Mode (100Mbps) - Data is not looped back. CRS is generated on transmit and collision detection is enabled.
- Loopback Test - Register bit 0.14 controls the MII loopback function. This capability is provided for diagnostics. Setting bit 0.14 = 1, causes the LXT970 to disconnect from the media interface and any data transmitted will be looped back to the receiver. No data will be sent or received from the media when this mode is enabled. When this diagnostic loopback is enabled, bit 0.7 can be used to test the operation of the COL pin.

MII Management Interface

The LXT970 supports the IEEE 802.3 MII Management Interface also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT970. MDIO interface consists of a physical connection, a specific protocol which runs across the connection, and an internal set of addressable registers. The physical interface consists of a data line (MDIO) and clock line (MDC), a control line (MDDIS) and an optional interrupt line (MDINT). The LXT970 can signal an interrupt using the MDIO signal as shown in Figure 3. The user can also assign a separate pin for this function. If Bit 17.1 = 1, pin 2 (FDS/MDINT) will be used as an MDINT pin.

Operation of this interface is controlled by the MDDIS input pin. When MDDIS is High, the MDIO operates as a read-only interface. When MDDIS is Low, read and write are enabled. The timing for the MDIO Interface is shown in Table 40. Read and write operations are shown in Figures 4 and 5. The protocol allows one controller to communicate with multiple LXT970 devices; each LXT970 is assigned an address between 0 and 31.

The LXT970 supports twelve 16-bit MDIO registers. Registers 0-7 are required and their functions are specified by the IEEE 802.3 specification. Additional registers are included for expanded functionality. The MDIO Register set for the LXT970 is described in Tables 43 through 54. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-31) and Y is the bit number (0-15).

Figure 3: MDIO Interrupt Signaling

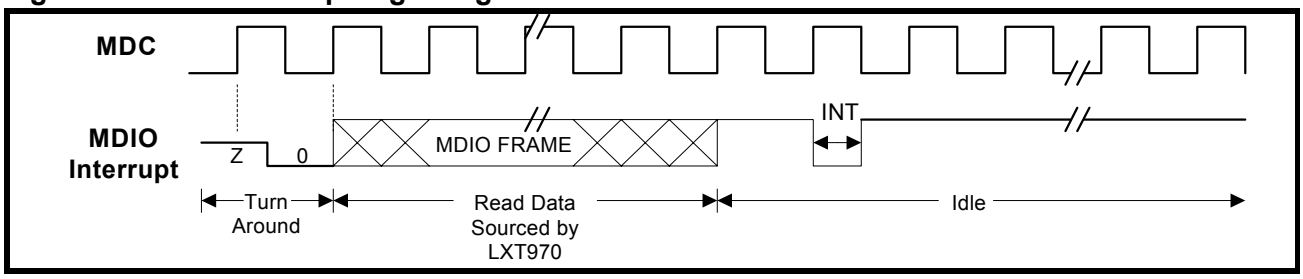


Figure 4: Management Interface - Read Frame Structure

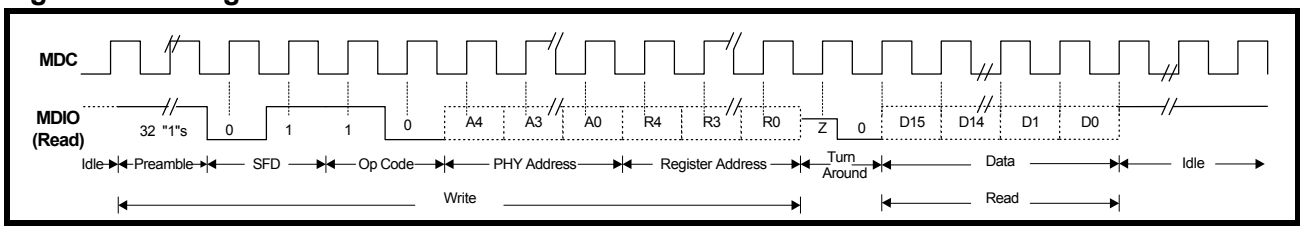
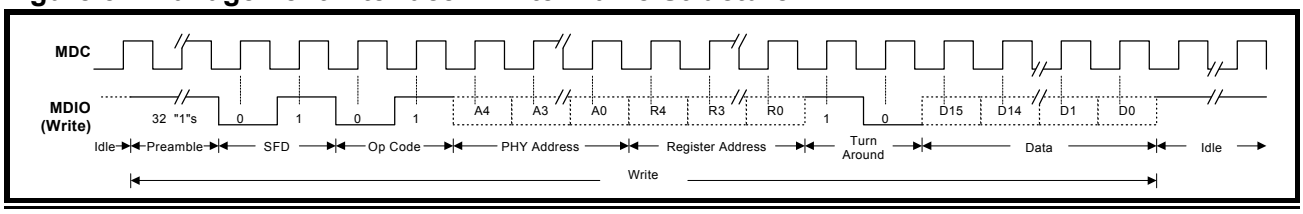


Figure 5: Management Interface - Write Frame Structure



Hardware Control Interface

The Hardware Control Interface consists of MF<4:0>, CFG <1:0> and FDE input pins. This interface is used to configure operating characteristics of the LXT970 and to determine the MDIO Address. When MDDIS is Low, the Hardware Control Interface provides initial values for the MDIO registers, and then passes control to the MDIO Interface.

When MDDIS is High, the Hardware Control Interface provides continuous control over the LXT970. Individual chip addressing allows multiple LXT970 devices to share the MII in either mode. Tables 10, 11 and 12 show how to set-up the desired operating configurations using the Hardware Control Interface.

Table 10: Configuring the LXT970 via Hardware Control

Desired Configuration	Pin Name	Input Value	MDIO Registers
Auto-Negotiation Enabled[1]	MF0	VMF2, VMF3	0.12 = 1
Auto-Negotiation Disabled[2]	MF0	VMF1, VMF4	0.12 = 0
Normal Operation (PHY Mode, Nibble Mode, Scrambler Enabled)	MF1 MF2 MF3	VMF1, VMF4	19.13 = 0 19.4 = 0 19.3 = 0
Repeater Mode	MF1	VMF2, VMF3	19.13 = 1
Symbol Mode	MF2	VMF2, VMF3	19.4 = 1
Scrambler Bypass Mode	MF3	VMF2, VMF3	19.3 = 1

1. Refer to Table 11 for Hardware Control Interface functions available when auto-negotiation is enabled.
2. Refer to Table 12 for Hardware Control Interface functions available when auto-negotiation is disabled.

Table 11: LXT970 Operating Configurations / Auto-Negotiation Enabled

Desired Configuration[1,2]	Pin Settings			MDIO Registers			
	MF4	CFG1	FDE	4.5	4.6	4.7	4.8
Advertise All	VMF1, VMF4	Low	Ignore	1	1	1	1
Advertise 100 HD	VMF2, VMF3	Low	Low	0	0	1	0
Advertise 100 HD/FD	VMF2, VMF3	Low	High	0	0	1	1
Advertise 10 HD	VMF1, VMF4	High	Low	1	0	0	0
Advertise 10 HD/FD	VMF1, VMF4	High	High	1	1	0	0
Advertise 10/100 HD	VMF2, VMF3	High	Low	1	0	1	0

1. Refer to Table 10 for basic configurations.
2. Refer to Table 12 for Hardware Control Interface functions available when auto-negotiation is disabled.

Table 12: LXT970 Operating Configurations / Auto-Negotiation Disabled

Desired Configuration[1,2]	Pin Name	Input Value	MDIO Registers
Force 100FX Operation	MF4	VMF2, VMF3	19.2 = 1
Force 100TX Operation	MF4	VMF1, VMF4	19.2 = 0
	CFG0	High	0.13 = 1
Force 10T Operation	MF4	VMF1, VMF4	19.2 = 0
	CFG0	Low	0.13 = 0
Force Full Duplex Operation	FDE	High	0.8 = 1
Disable 10T Link Test	CFG1	High	19.8 = 1
Enable 10T Link Test	CFG1	Low	19.8 = 0

1. Refer to Table 10 for basic configurations.
2. Refer to Table 11 for Hardware Control Interface functions available when auto-negotiation is enabled.

Initialization

At power-up or reset, the LXT970 performs the initialization as shown in Figure 6. When pin 15 (MDDIS) is High, the LXT970 enters Manual Control Mode. When MDDIS is Low, MDIO Control Mode is enabled. Mode control selection is provided via the MDDIS pin as shown in Table 13.

MDIO Control Mode

In the MDIO Control mode, the LXT970 uses the Hardware Control Interface to set up initial (default) values of the MDIO registers. Once initial values are set, bit control reverts to the MDIO interface.

Manual Control Mode

In the Manual Control Mode, LXT970 disables direct write operations to the MDIO registers on the MDIO interface. The Hardware Control Interface is continuously monitored and the MDIO registers are updated accordingly.

Table 13: Mode Control Settings

MDDIS Pin 15	RESET Pin 16	PWRDWN Pin 34	Mode
Low	High	Low	MDIO Control
High	High	Low	Manual Control
-	Low	Low	Reset
-	-	High	Power Down

Link Configuration

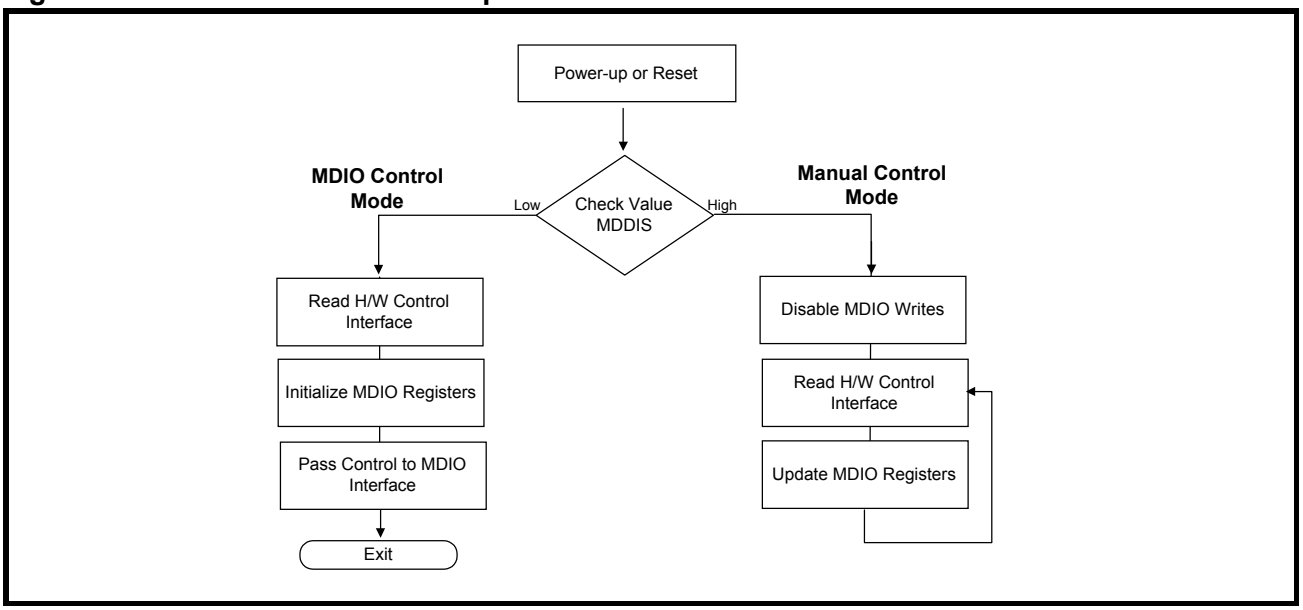
When the LXT970 is first powered on, reset, or encounters a link failure state, it must determine the line speed and operating conditions to use for the network link.

The LXT970 first checks the MDIO registers (initialized via the Hardware Control Interface or software) for operating instructions. Using these mechanisms, the user can command the LXT970 to do one of the following:

- Force 100FX (Fiber)
- Force twisted-pair link operation to:
  - 100TX, Full Duplex
  - 100TX, Half Duplex
  - 10BASE-T, Full Duplex
  - 10BASE-T, Half Duplex
- Allow auto-negotiation/parallel-detection.

In the first two cases, the LXT970 immediately begins operating the network interface as commanded. In the third case, the LXT970 begins the auto-negotiation/parallel-detection operation.

Figure 6: LXT970 Initialization Sequence



Auto-Negotiation

At power-up or reset, with auto-negotiation enabled, the LXT970 attempts to establish link operating conditions with its partner by sending FLP (Fast Link Pulse) bursts. By exchanging FLP bursts, the LXT970 and its link partner communicate their capabilities to each other. Each side finds the highest common capabilities that both sides can support and then begins operating in that mode.

Parallel Detection

In parallel with auto-negotiation, the LXT970 also checks for 10 Mbps Normal Link Pulses (NLP) or 100 Mbps Idle symbols. If either is detected, the device automatically configures to match the detected operating speed in half duplex mode. This ability allows the LXT970 to communicate with devices that do not support auto-negotiation.

Controlling Auto-Negotiation

When auto-negotiation is controlled by software, the following steps are recommended:

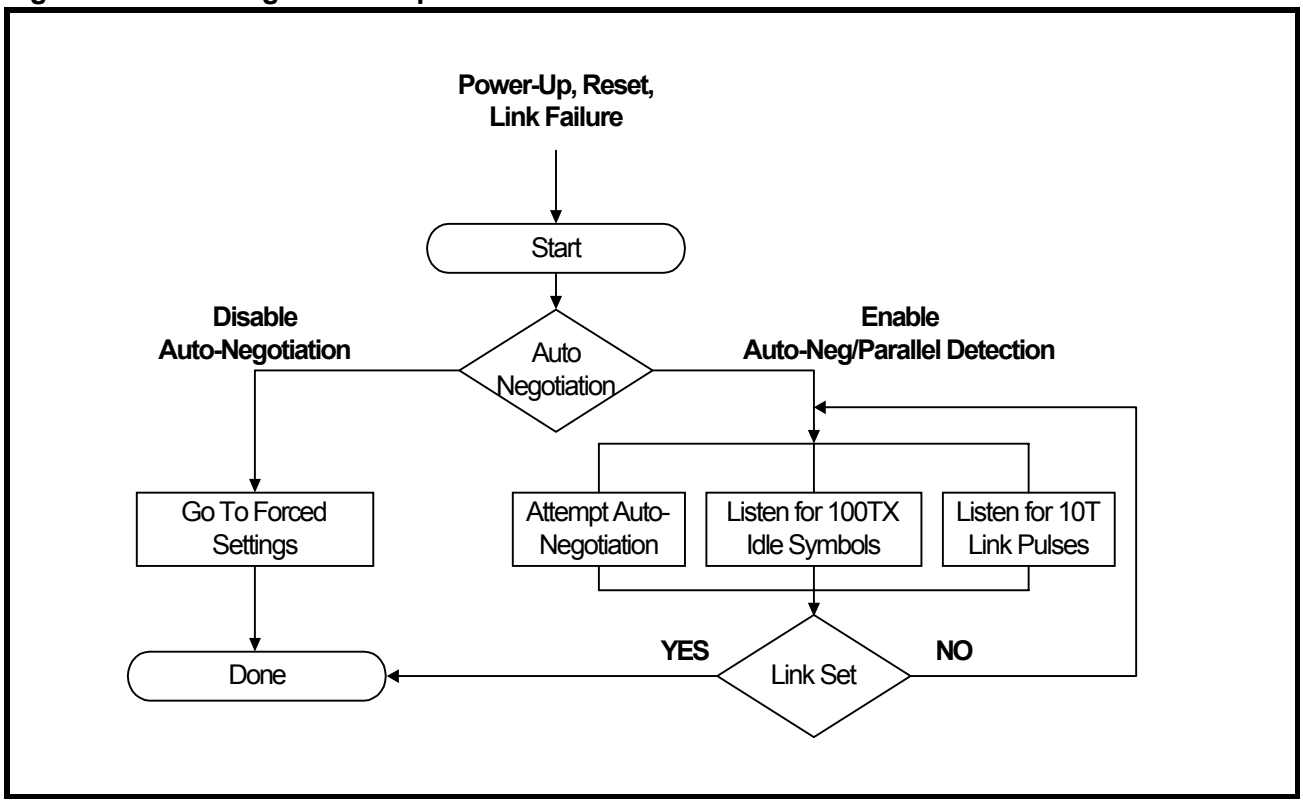
- After power-up, power down, or reset, the power down recovery time, as specified in Table 41, must be exhausted before proceeding.
- Set MDIO Register 4 advertisement capabilities before enabling auto-negotiation by setting MDIO bit 0.12 = 1

Monitoring Auto-Negotiation

When auto-negotiation is being monitored, the following apply:

- Bit 20.13 is set to 1 once the link is established
- Bits 20.12 and 20.11 can be used to determine the link operating conditions (speed and duplex)
- Operation can be forced by disabling auto-negotiation (bit 0.12 = 0) and setting bits 0.13, 0.8 and 19.2

Figure 7: Auto-Negotiation Operation



100 Mbps Operation

The MAC transmits data to the LXT970 over the MII. In 100BASE-TX mode, the LXT970 encodes and scrambles the data, then transmits it using MLT-3 signalling. The LXT970 descrambles and decodes MLT-3 data received from the network. In 100BASE-FX mode, the LXT970 transmits and receives data as NRZI signals.

When the MAC is not actively transmitting data, the LXT970 sends out Idle symbols on the line.

As shown in Figure 8, the MAC starts each transmission with a preamble pattern. When TX_EN is asserted, the LXT970 transmits a J/K symbol to the network (Start of Stream Delimiter or SSD). It then encodes and transmits the rest of the packet, including the balance of the preamble, the SFD (Start of Frame Delimiter), packet data, and CRC. Once the packet ends, the LXT970 transmits the T/R symbol (End of Stream Delimiter or ESD) and then returns to transmitting Idle symbols.

Normally, 4-bit wide nibble data is transmitted across the MII interface and RXD4/TXD4 are ignored. The encoder translates the 4-bit nibbles into 5-bit symbols which are sent over the 100BASE-X connection. In Symbol Mode, a fifth bit is provided (RXD4/TXD4) to allow a 5-bit symbol to be sent across the MII interface.

Figure 9 shows the data conversion flow from nibbles to symbols. Table 14 shows 4B/5B symbol coding. Note that some symbols are invalid.

Figure 8: 100BASE-TX Frame Structure

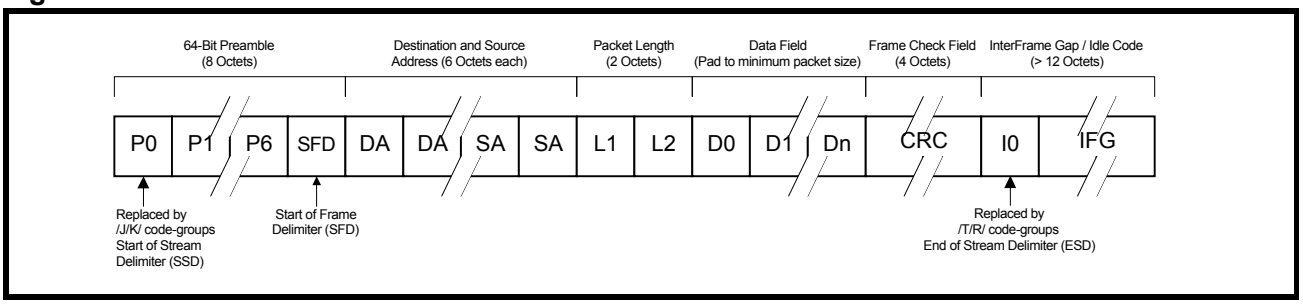


Figure 9: 100BASE-TX Data Flow

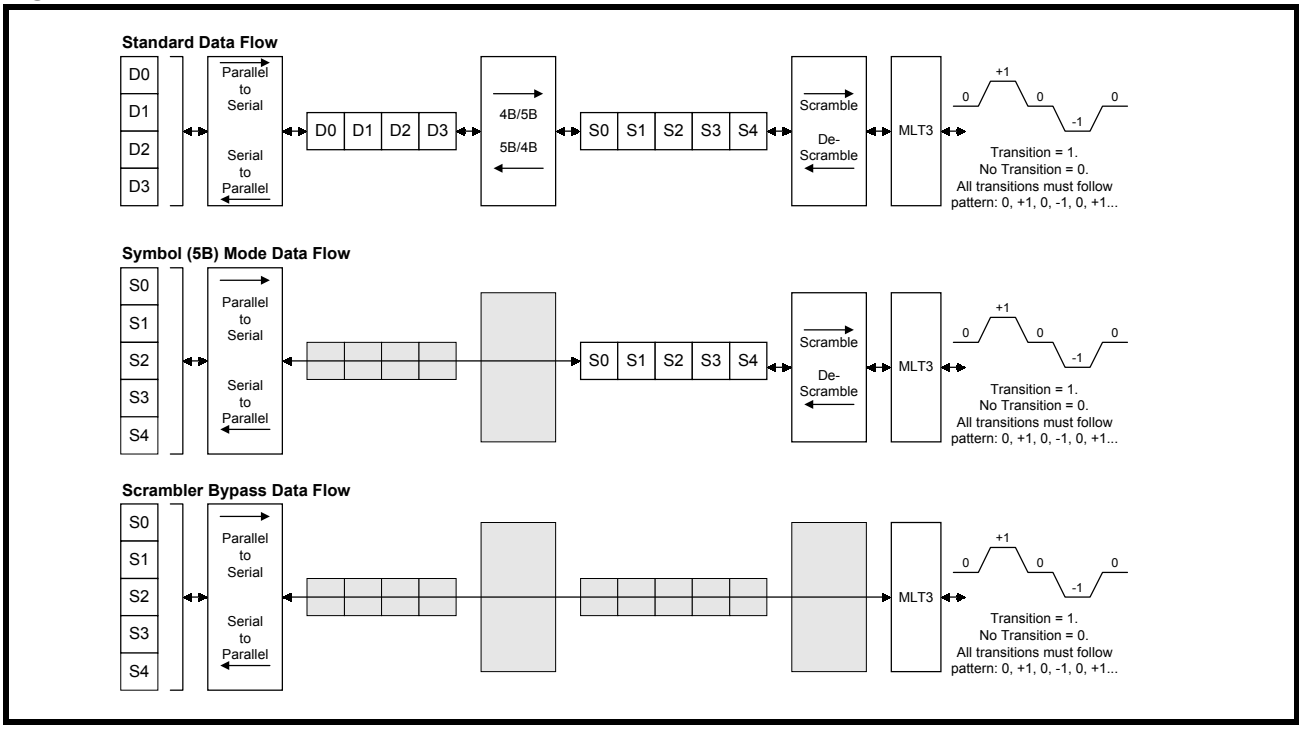


Table 14: 4B/5B Coding

Code Type	4B Code 3 2 1 0	Name	5B Symbol 4 3 2 1 0	Interpretation
DATA	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5
	0 1 1 0	6	0 1 1 1 0	Data 6
	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E
	1 1 1 1	F	1 1 1 0 1	Data F
IDLE	undefined	I [1]	1 1 1 1 1	Idle. Used as inter-stream fill code
CONTROL	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2
	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2
	undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (SSD), part 1 of 2
	undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (SSD), part 2 of 2
INVALID	undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signaling errors
	undefined	Invalid	0 0 0 0 0	Invalid
	undefined	Invalid	0 0 0 0 1	Invalid
	undefined	Invalid	0 0 0 1 0	Invalid
	undefined	Invalid	0 0 0 1 1	Invalid
	undefined	Invalid	0 0 1 0 1	Invalid
	undefined	Invalid	0 0 1 1 0	Invalid
	undefined	Invalid	0 1 0 0 0	Invalid
	undefined	Invalid	0 1 1 0 0	Invalid
	undefined	Invalid	1 0 0 0 0	Invalid
	undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code-group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code-groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code-groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code-group is used to signal an error condition.

5B Symbol Mode

In Symbol Mode, raw 5-bit symbol data is passed directly across the MII interface and the encoder is bypassed. Symbol Mode is selected by setting bit 19.4 = 1 or by setting input pin MF2 = VMF2 or VMF3.

This mode reduces device latency for use in repeater applications. See Table 31 and 32 for timing parameters.

Scrambler Seeding

Once the transmit data (or Idle symbols) are properly encoded, they are scrambled to further reduce EMI and to spread the power spectrum using an 11-bit scrambler seed. Ten seed bits are determined by MF<4:0> inputs and LED outputs, and one bit is randomly determined.

Scrambler Bypass

The scrambler/descrambler can be bypassed by either setting bit 19.3 = 1 or setting input pin MF3 to VMF2/VMF3. The scrambler is automatically bypassed when the fiber port is enabled. Symbol Mode (5B) must also be enabled for the LXT970 to work properly while in Scrambler Bypass Mode. Scrambler Bypass is provided for diagnostic and test support.

Link Failure

Link failure is declared when an excessive number (250 out of 1000) of invalid symbols are received. The LXT970 reports link failure via the MII status bits (1.2, 18.15 and 20.13) and interrupt functions. If auto-negotiation is enabled, link failure causes the LXT970 to re-negotiate.

Link Failure Override

The LXT970 will normally transmit 100Mbps data packets only if it detects the link is up, and transmits only Idle symbols or FLP bursts if the link is not up. Setting bit 19.14 = 1 overrides this function, allowing the LXT970 to transmit data packets even when the link is down. This feature is provided as a diagnostic tool. Note that auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT970 will automatically begin transmitting FLP bursts if the link goes down.

Baseline Wander Correction

The LXT970 provides a baseline wander correction function which makes the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is by definition “unbalanced”. This means that the DC average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). This wander can cause receiver errors, particularly at long line lengths (100 meters). The exact characteristics of the wander are completely data dependent. “Killer Packets” have been created that exhibit worst case baseline wander characteristics. The LXT970 baseline wander correction characteristics allow the LXT970 to recover error-free data, even at long line lengths.

FX Operation

To enable 100BASE-FX operation, auto-negotiation must be disabled and FX selected.

- To disable auto-negotiation, set 0.12 = 0, or set MF0 = VMF1 or VMF4.
- To select FX, set 19.2 = 1, or set MF4 = VMF2 or VMF3.

In FX mode, the following conditions apply:

- CFG0 / 0.13 still controls speed and must be set to 1 for 100 Mbps operation.
- Scrambler is automatically disabled.
- 5-bit symbol mode may be selected by setting 19.4 = 1, or setting MF2 = VMF2 or VMF3.
- Duplex operation is controlled by pin FDE or by bit 0.8.

Data Errors

Figure 10 shows normal reception. When the LXT970 receives invalid symbols from the line, it asserts RX_ER, as shown in Figure 11.

Collision Indication

Figure 12 shows normal transmission. The LXT970 detects a collision if transmit and receive are active at the same time. As shown in Figure 13, upon detection of a collision, the COL output is asserted and remains asserted for the duration of the collision.

Figure 10: 100BASE-TX Reception with No Errors

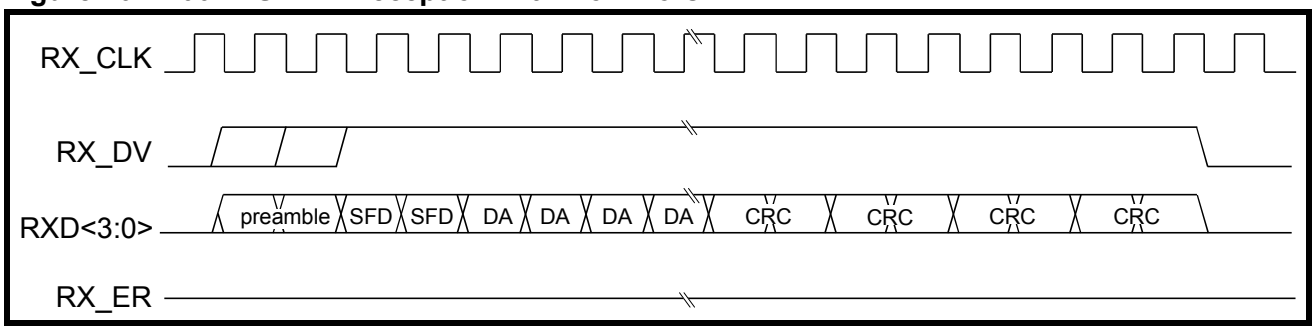


Figure 11: 100BASE-TX Reception with Invalid Symbol

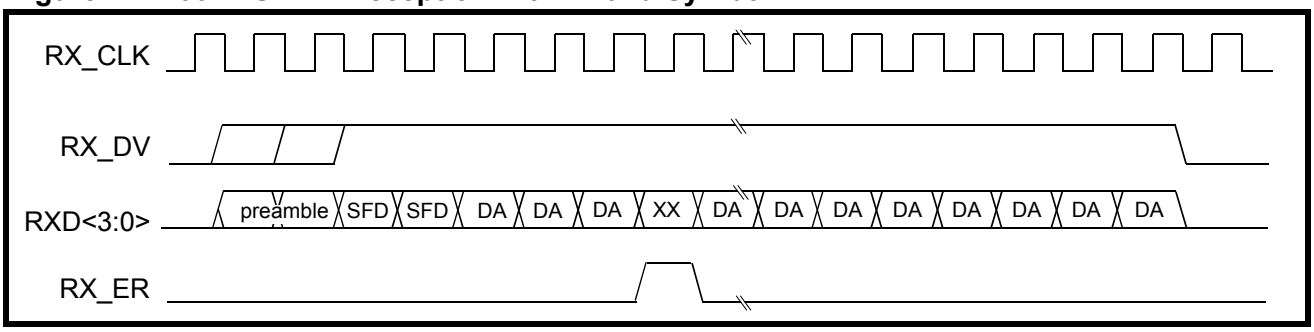


Figure 12: 100BASE-TX Transmission with No Errors

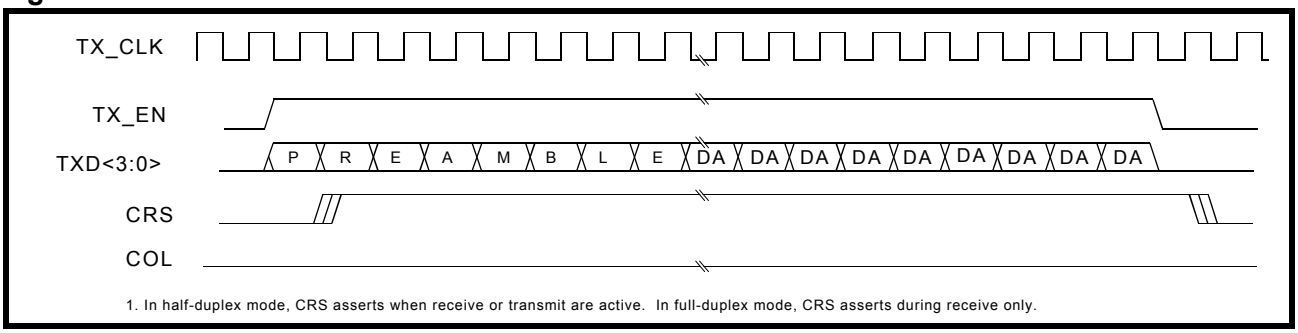
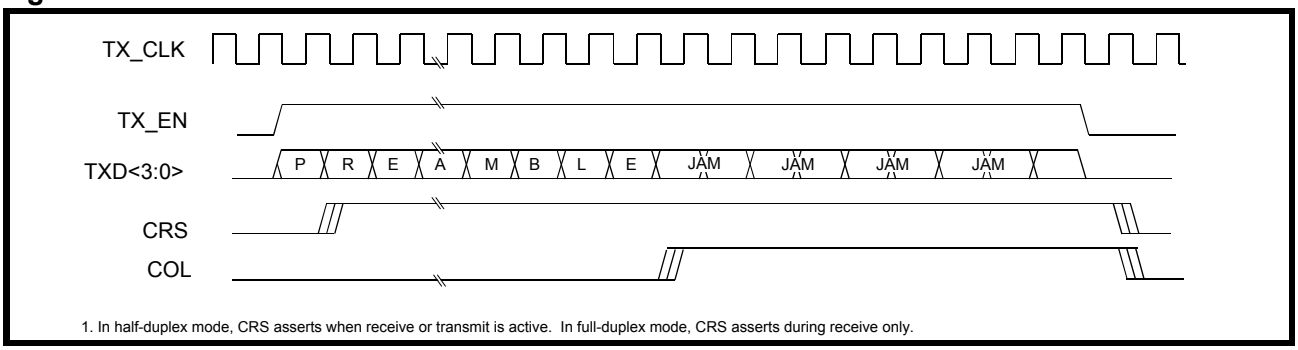


Figure 13: 100BASE-TX Transmission with Collision



10 Mbps Operation

The LXT970 will operate as a standard 10 Mbps transceiver. Data transmitted by the MAC as 4-bit nibbles is serialized, Manchester-encoded, and transmitted on the TPOP/N outputs. Received data is decoded, de-serialized into 4-bit nibbles and passed to the MAC across the MII. The LXT970 supports all the standard 10Mbps functions.

Link Test

In 10 Mbps mode, the LXT970 always transmits link pulses. If the Link Test Function is enabled, it monitors the connection for link pulses. Once it detects 2 to 7 link pulses, data transmission will be enabled and will remain enabled as long as the link pulses or data transmission continues. If the link pulses stop, the data transmission will be disabled.

If the Link Test function is disabled, the LXT970 will transmit to the connection regardless of detected link pulses. The Link Test function can be disabled by setting Bit 19.8 = 1 or by setting MF0 to disable auto-negotiation and setting CFG1 input High.

SQE (Heartbeat)

By default, the SQE (heartbeat) function is disabled on the LXT970. To enable this function, set bit 19.10 = 1. When this function is enabled, the LXT970 will assert its COL output for 5-15 BT after each packet. See Figure 24 for SQE timing parameters.

Jabber

If the MAC begins a transmission that exceeds the jabber timer, the LXT970 disables the transmit and loopback functions and enables the COL pin. The LXT970 automatically exits jabber mode after 250-750ms. This function can be disabled by setting Bit 19.9 = 1. See Figure 25 for Jabber timing parameters.

Polarity Correction

The LXT970 automatically detects and corrects for the condition where the receive signal (TPIP/N) is inverted. Reversed polarity is detected if 8 inverted link pulses, or 4 inverted end-of-frame markers, are received consecutively. If link pulses or data are not received for 96-128 ms, the polarity state is reset to a non-inverted state.

Link Failure

Link failure occurs if Link Test is enabled and link pulses stop being received. If this condition occurs, the LXT970 returns to the auto-negotiation phase if auto-negotiation is enabled.

Operating Requirements

Power Requirements

The LXT970 requires four +5V supply inputs (VCCA, VCCD, VCCR and VCCT). These inputs may be supplied from a single source although decoupling is required to each respective ground. As a matter of good practice, these supplies should be as clean as possible. Typical filtering and decoupling are shown in the Application Information section, Figure 15. An additional supply is required for the MII (VCCIO). The MII supply may be either +5V or +3.3V. Power for the MII should be supplied from the same power source used for the controller on the other side of the MII interface.

Low Voltage Fault Detect

The LXT970 has a low voltage fault detection function that prevents transmission of invalid symbols when VCC goes below normal operating levels. This function disables the transmit outputs when a low voltage fault on VCC occurs. If this condition happens, the LXT970 sets 20.2 = 1. Operation is automatically restored when VCC returns to normal. Table 24 indicates voltage levels used to detect and clear the low voltage fault condition.

Power Down Mode

The LXT970 goes into Power Down Mode when PWRDWN is asserted. In this mode, all functions are disabled except the MDIO. The power supply current is significantly reduced. Refer to Table 19 for power down specifications. This mode can be used for energy-efficient applications or for redundant applications where there are two devices and one is left as a stand-by. When the LXT970 is returned to normal operation, configuration settings of the MDIO registers are maintained.

Clock Requirements

The LXT970 requires a constant clock that must be enabled at all times. Depending on the mode of operation, the clock may be supplied at the crystal oscillator pins (XI, XO), or at the Transmit Clock pin (TX_CLK). There are two clock modes, master clock mode and slave clock mode. See Table 23 for input clock requirements.

Master Clock Mode

The Master Clock mode is recommended in most Network Interface Cards (NICs) and switch applications. In the Master Clock mode the LXT970 is the master clock source for data transmission, and requires a 25 MHz reference signal at XI.

In master clock mode, TX_CLK is an output and the LXT970 automatically sets the speed of TX_CLK to match line conditions. If the line is operating at 100Mbps, TX_CLK will be set to 25MHz. If the line is operating at 10Mpbs, TX_CLK will be set to 2.5MHz.

External Crystal

An external 25 MHz crystal connected across XI and XO is recommended to supply the LXT970 internal clock reference. A crystal is typically used in NIC applications.

External Clock

An external 25 MHz clock source, rather than a crystal, is frequently used in switch applications. When a clock is supplied to XI, XO is left open.

TX Clock Advance Mode

When operating in Master Clock mode under MDIO Control, the user can advance the transmit clock relative to TXD<4:0> and TX_ER. This option can be used to compensate for propagation delays in applications with long MII cables. When TX_CLK Advance is selected, the LXT970 clocks TXD data in on the falling edge of TX_CLK, instead of the rising edge. This mode provides an increase in timing margins of TXD, relative to TX_CLK. TX_CLK Advance is enabled when bit 19.5 = 1.

Slave Clock Mode

The Slave Clock mode is typically used for repeater applications, where the LXT970 is not the master clock source for data transmissions.

In slave clock mode, the application circuit must drive TX_CLK in accordance with the line conditions. A frequency of 25MHz will support a line rate of 100Mbps only. A clock frequency of 2.5MHz will only support a line rate of 10Mbps. Either speed can be used during auto-negotiation. In Slave Clock mode XI is connected to ground and XO is left open.

APPLICATION INFORMATION

Magnetics Information

The LXT970 requires a 1:1 ratio for both the receive and the transmit transformers. Refer to Table 16 for transformer requirements. Transformers meeting these requirements are available from various manufacturers. Designers should test and validate all magnetics before using them in production.

Crystal Information

Refer to Table 17 for crystal requirements. Crystals are available from various manufacturers. Designers should test and validate all crystals before committing to a specific component.

Component Manufacturers.

Based on limited evaluations, Table 15 provides a list of suitable components and manufacturers.

Table 15: Component Manufacturers

Component	Manufacturer	Part Number
Magnetics	Halo	TG22-3506ND
		TD22-3506G1
		TG22-S010ND
		TG22-S012ND
	Nanopulse	NPI 6120-30
		NPI 6120-37
		NPI 6170-30
		NPI 6181-37
	Pulse	PE-68517
		PE-68515
	Valor	ST6114
		ST6118
Crystals	CTS	CTX093
	Epson America	SE2539CT

Table 16: Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Turns Ratio	–	1:1	–	–	
Insertion Loss	0.0	–	0.6	dB	
Primary Inductance	350	–	–	µH	
Transformer Isolation	–	2	–	kV	
Differential to common mode rejection	40	–	–	dB	.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	17	–	–	dB	.1 to 60 MHz
	15	–	–	dB	60 to 100 MHz
Rise Time	2.0	–	3.5	ns	10% to 90%

Table 17: Crystal Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Frequency	–	25.0	–	MHz	
Frequency Stability	–	–	±100	ppm	-40 - 85°C

1. See Table 23 (Clock Characteristics) for additional device specifications.

Layout Requirements

The Twisted Pair Interface

The layout of the twisted-pair ports is critical in complex high-speed designs. Careful planning during the schematic and layout stages of the design will minimize these problems.

General Twisted-Pair Interface Layout Considerations

- The transformer isolation voltage should be rated at 2kV to protect the circuitry from static voltages across the connectors and cables.
- Place the transformer as close as possible to the connector.
- The traces running from the transformer to the connector should run in close pairs directly to the connector.
- Be careful not to cross the transmit and receive pairs.
- Vias should be avoided as much as possible.

Ground Plane Layout Considerations

Ground plane layout depends on the availability and quality of chassis ground. If a solid chassis ground is not available, there should be no power or ground planes in the area between the LXT970, the transformers and the connectors. High frequency noise on these planes causes interference on the data signals and induces EMI emissions. The data signals should be the only traces in this area, except for the termination of unused pairs or LEDs.

If a solid and quiet chassis ground is available that is well-decoupled from the active power and ground planes, it can be routed under the twisted pair signal traces to reduce EMI emissions. Position chassis ground at the edge of the board, encircling the PCB. Separate chassis ground from the digital and analog ground planes with an isolating moat and connect them through inductors. Keep chassis ground away from all active signals. If required, the RJ45 connector and any unused pins can be tied to chassis ground through a resistor divider network and a 2kV bypass capacitor.

The RBIAS Pin

The RBIAS pin sets the levels for the LXT970 output drivers. Any emissions or common mode noise entering the device here could be measured on the twisted pair output signals.

The LXT970 requires a 22kΩ, 1% resistor directly connected between the RBIAS pin and ground. This resistor should be as close to the device as possible and the traces should be as short as possible. Keep all high speed signals away from the RBIAS pin. The ground traces from adjacent pin GNDA should come directly off of the device to enclose the resistor and pin forming a shielded area between the RBIAS connection and the switching signals on the PCB.

Power Supply Decoupling

Ferrite Beads

Ferrite beads are recommended for decoupling the analog and digital supplies. The ferrite bead used should have an impedance of at least 100Ω at 100MHz. A suitable bead is the Panasonic surface mount bead, part number EXCCL4532U, or equivalent. For all applications,

- GNDT should be connected directly to GNDA.
- VCCT and VCCA should be connected and isolated from VCCD by a ferrite bead.
- For long line length performance (>120 meters), beads may be installed between VCCT and VCCR and between GNDT and GNDR. These beads are not required for applications <120 meters.
- Depending on the application, a ferrite bead may be required between GNDT/GNDA and GNDD. See explanation below.

For applications where the digital ground plane is noisy, a ferrite bead between GNDT/GNDA and GNDD may be required to prevent noise interference. If the digital ground plane is quiet, this ground bead may not be required.

Bypass Caps

Bypass caps are required between each supply and its associated ground return (VCCA/GNDA, VCCR/GNDR, VCCT/GNDT, VCCD/GNDD and VCCIO/GNDIO). The recommended cap is 0.1µF or .01µF, as required by the design layout.

10µF tantalum caps are recommended between VCCA and GNDA and between VCCD and GNDD on both sides of the ferrite beads.

For long line applications, when ferrite beads are used between the transmit and receive supplies and grounds, a tantalum cap is required on the device side of the ferrite bead between GNDR and VCCR.

If a crystal is used, it should be bypassed to GNDD.

The Fiber Interface

In fiber-only applications, reference the fiber ports to the analog power and ground planes (VCCA, GNDA, VCCT, GNDT, VCCR, GNDR). In a combination fiber and twisted-pair application, reference the fiber ports to the digital power and ground planes (VCCD, GNDD). In applications where the fiber interface is not used, the fiber I/O pins (FIBIP/N and FIBOP/N) may be left unconnected

Typical Application

Figure 15 is a typical application of the LXT970. The diagram groups similar pins; it does not portray the actual chip pinout. The Media Independent Interface pins are at the upper left. Hardware Control Interface pins are center left. The line interface pins for twisted-pair and fiber are shown on the top and bottom right respectively.

The VCCD and VCCIO pins are at the bottom of the diagram. VCCT, VCCR and VCCA are at the center right. All VCC pins (except VCCIO) use a single power supply. VCCIO may be powered by a 3.3V supply, and may be separately connected.

Voltage Divider For MF Inputs

The LXT970 requires an external voltage divider to provide optional ($V_{MF}2$ and $V_{MF}3$) multi-level inputs to the Multi-Function (MF) pins. These voltage levels are designated as $V_{MF}1$ - $V_{MF}4$. Figure 14 shows a voltage divider with three 1kΩ resistors configured in series between VCC and Ground.

Figure 14: Voltage Divider

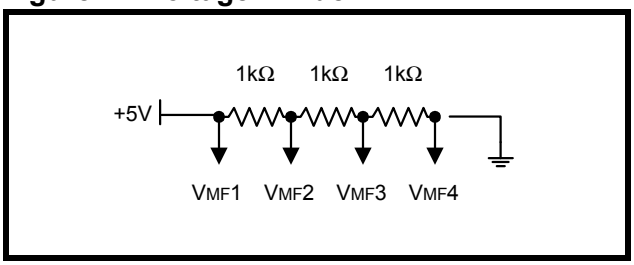
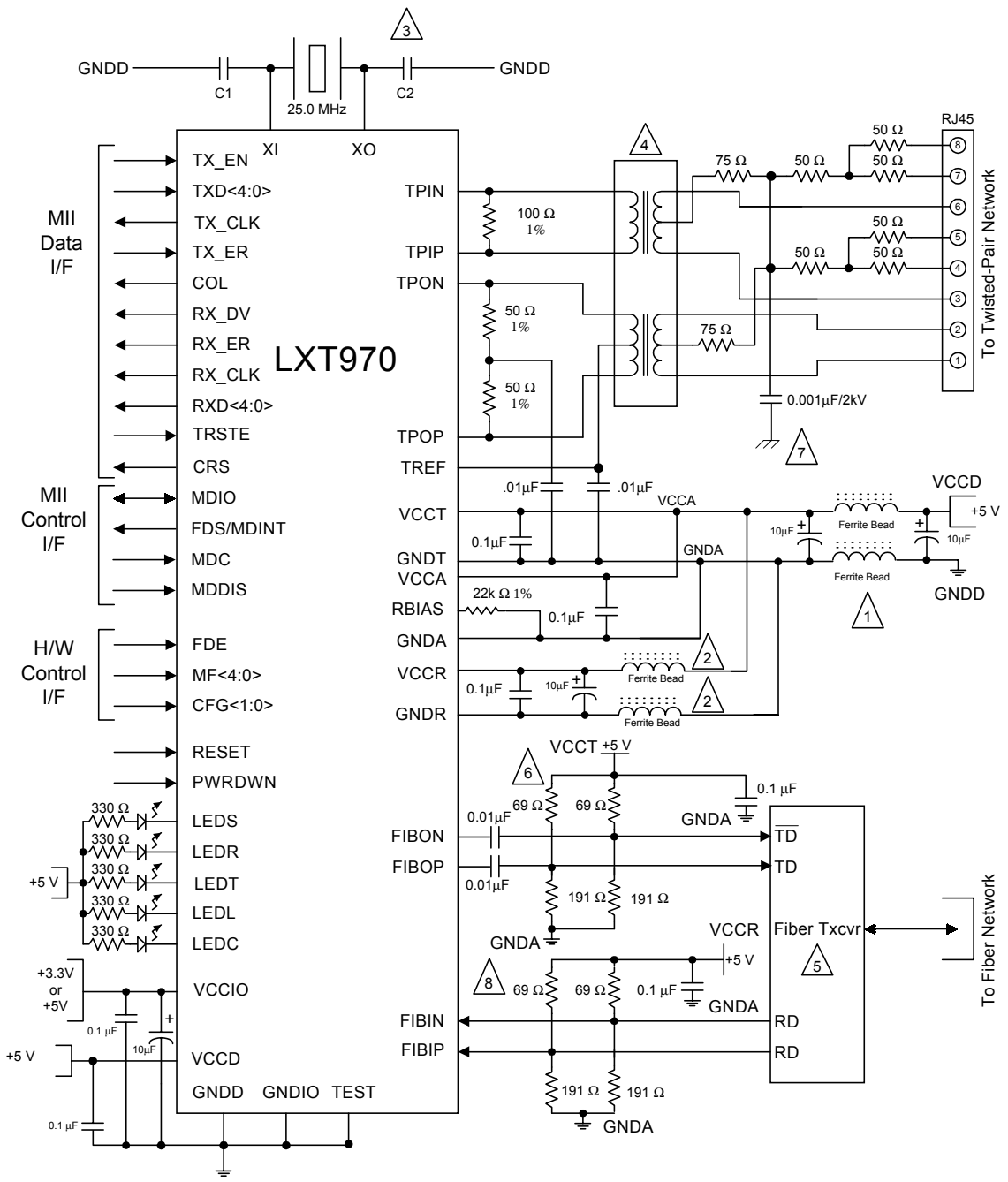


Figure 15: Typical Network Interface Card (NIC) Application



1. This ferrite bead is suggested for applications with noisy ground planes.
2. These beads may improve long line length performance (>120 meters), but not required for applications <120 meters.
3. Refer to Tables 15 and 17 for crystals.
4. Refer to Tables 15 and 16 for magnetics.
5. Refer to fiber transceiver manufacturers recommendations for termination circuitry. Suitable fiber transceivers include the HFBR-5103 and HFBR-5105.
6. Suggested supply layout for fiber-only applications. In combination twisted-pair and fiber applications, use VCCD/GNDD.
7. Bypassing to chassis ground (if available) provides additional EMI shielding.
8. If the Fiber Interface is not used, FIBIN, FIBIP, FIBON and FIBOP may be left unconnected.

TEST SPECIFICATIONS

Note

Minimum and maximum values in Tables 18 through 41 and Figures 16 through 30 represent the performance specifications of the LXT970 and are guaranteed by test except, where noted, by design.

Table 18: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
Supply Voltage	VCC	-0.3	6	V
Operating Temperature	TOP	-15	+85	ºC
Storage Temperature	TST	-65	+150	ºC

CAUTION

Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19: Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Recommended Supply Voltage[2]	Except MII Supply	VCC	4.75	5.0	5.25	V	
	MII Supply	VCCIO	3.125	–	5.25	V	
Recommended Operating Temperature		TOP	0	–	70	ºC	
VCC Current (+5V Only)	100BASE-TX	ICC	–	170	–	mA	
	100BASE-FX	ICC	–	80	–	mA	
	10BASE-T	ICC	–	185	–	mA	
	Power Down Mode	ICC	–	9	–	mA	
	Auto-Negotiation	ICC	–	240	270	mA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.

Table 20: Digital I/O Characteristics[1] - (Over Recommended Range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage[3]	V_{IL}	–	–	0.8	V	
Input High voltage[3]	V_{IH}	2.0	–	–	V	
Input Current	I_I	-10	–	10	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

1. Applies to all pins except MII and MF<4:0> pins. Refer to Table 21 for MF pin I/O Characteristics and Table 22 for MII I/O Characteristics.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. Does not apply to XI or TX_CLK pins. Refer to Table 23 for clock input levels.

Table 21: Digital I/O Characteristics - MultiFunction Pins MF<4:0> (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Voltage Level 1	V_{MF1}	V_{CC} - 0.5	–	–	V	
Input Voltage Level 2	V_{MF2}	(V_{CC}/2) + 0.5	–	V_{CC} - 1.2	V	
Input Voltage Level 3	V_{MF3}	1.2	–	V_{CC}/2 - 0.5	V	
Input Voltage Level 4	V_{MF4}	–	–	0.5	V	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 22: Digital I/O Characteristics - MII Pins (Over Recommended Range)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	.8	V	
Input High voltage	V_{IH}	2.0	–	–	V	
Input Current	I_I	-10	–	10	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.2	–	–	V	I_{OH} = -4 mA, V_{CCIO} = 3.3V
	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA, V_{CCIO} = 5.0V
Driver Output Resistance (Line driver output enabled)	R_O[1]	6.0	–	25.0	Ω	V_{CCIO} = 3.3V
	R_O[1]	6.0	–	25.0	Ω	V_{CCIO} = 5.0V

1. Parameter is guaranteed by design; not subject to production testing.

Table 23: Required Clock Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Master Clock Mode - External XI Clock Input						
Input Low Voltage[2]	VIL	–	–	1.0	V	
Input High Voltage[2]	VIH	3.2	–	–	V	
Input Clock Frequency Tolerance[2]	Δf	–	–	± 100	ppm	Clock frequency is 25 MHz or 2.5 MHz
Input Clock Duty Cycle[2]	TDC	40	–	60	%	
Input Capacitance (XI and XO)	CIN	–	3.0	–	pF	
Slave Clock Mode - External TX_CLK Input						
Input Low Voltage	VIL	–	–	.8	V	
Input High Voltage	VIH	2.0	–	–	V	
Input Clock Frequency Tolerance[2]	Δf	–	–	± 100	ppm	Clock frequency is 25 MHz or 2.5 MHz
Input Clock Duty Cycle[2]	TDC	35	–	65	%	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

Table 24: Low Voltage Fault Detect Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Detect Fault Threshold	VLT	3.4	–	4.0	V	–
Clear Fault Threshold	VLH	4.1	–	4.7	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 25: 10BASE-T Link Integrity Timing Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Time Link Loss Receive	TLL	50	64	150	ms	–
Link Pulse	TLP	2	4	7	Link Pulses	–
Link Min Receive Timer	TLR MIN	2	4	7	ms	–
Link Max Receive Timer	TLR MAX	50	64	150	ms	–
Link Transmit Period	TLT	8	10	24	ms	–
Link Pulse Width	TLPW	–	100	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 26: 100BASE-TX Transceiver Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	VOP	0.95	–	1.05	V	Note 2
Signal amplitude symmetry	Vss	98	–	102	%	Note 2
Signal rise/fall time	TRF	3.0	–	5.0	ns	Note 2
Rise/fall time symmetry	TRFS	–	–	0.5	ns	Note 2
Duty cycle distortion	DCD	–	–	± 0.5	ns	Offset from 16ns pulse width at 50% of pulse peak
Overshoot/Undershoot	VOS	–	–	5	%	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the specified transformer, line replaced by 100Ω (±1%) resistor.

Table 27: 100BASE-FX Transceiver Characteristics (Over Recommended Range**)**

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak Differential Output Voltage (single ended)	VOP	0.6	–	1.0	V	–
Signal rise/fall time	TRF	–	–	1.6	ns	10 <–> 90% 2.0 pF load
Jitter (measured differentially)	–	–	–	1.3	ns	–
Receiver						
Peak Differential Input Voltage	VIP	0.55	–	1.5	V	–
Common Mode Input Range	VCMIR	2.25	–	VCC - 0.5	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 28: 10BASE-T Transceiver Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak Differential Output Voltage	VOP	2.2	2.5	2.8	V	With specified transformer, line replaced by 100Ω (±1%) resistor
Transmit timing jitter added by the MAU and PLS sections[2,3]	–	0	2	11	ns	After line model specified by IEEE 802.3 for 10BASE-T MAU
Receiver						
Receive Input Impedance[2]	ZIN	–	3.6	–	kΩ	Between TPIP/TPIN
Differential Squelch Threshold	VDS	300	420	585	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 1.5ns for the AUI cable, 0.5ns from the encoder, and 3.5ns from the MAU.

Figure 16: MII - 100BASE-TX Receive Timing / 4B Mode

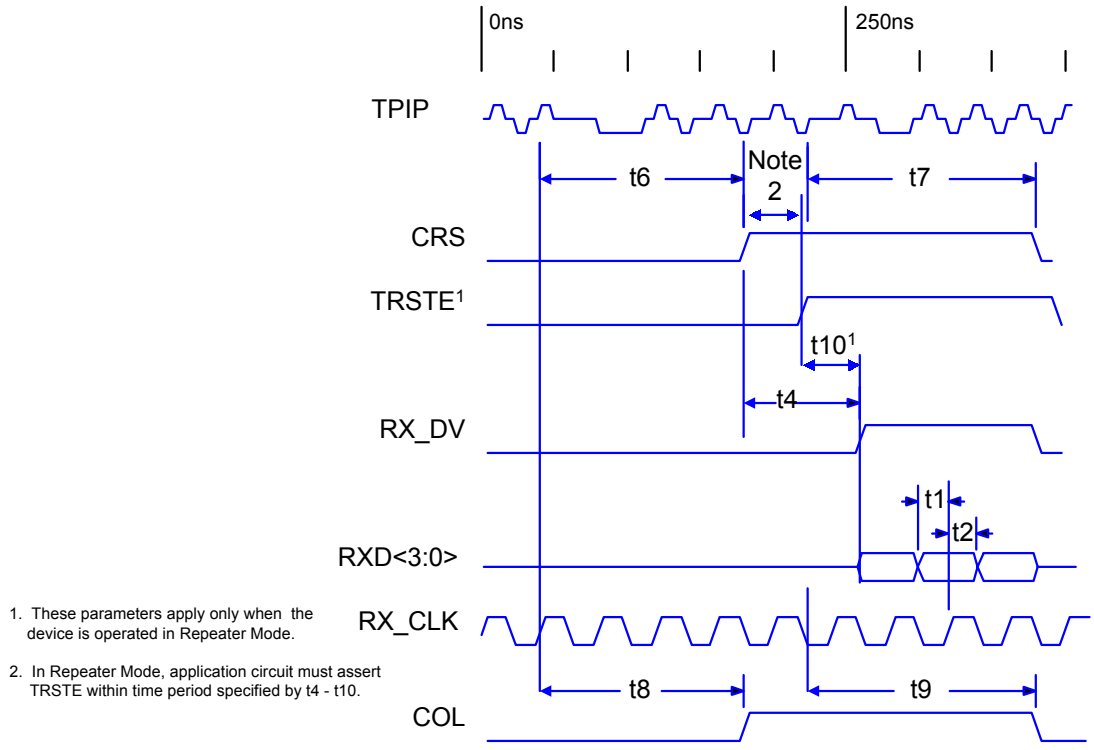


Table 29: MII - 100BASE-TX Receive Timing Parameters / 4B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	10	–	–	ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	5	–	–	ns
CRS asserted to RXD<3:0>, RX_DV asserted	t4	–	8	–	BT
Receive start of "J" to CRS asserted	t6	0	15 - 19	20	BT
Receive start of "T" to CRS de-asserted	t7	13	23 - 27	28	BT
Receive start of "J" to COL asserted	t8	0	15 - 19	20	BT
Receive start of "T" to COL de-asserted	t9	13	23 - 27	28	BT
TRSTE asserted to RX_DV, RXD<3:0> driven[2]	t10	–	20	–	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. These parameters apply only when the device is operated in Repeater Mode.

Figure 17: MII - 100BASE-TX Transmit Timing / 4B Mode

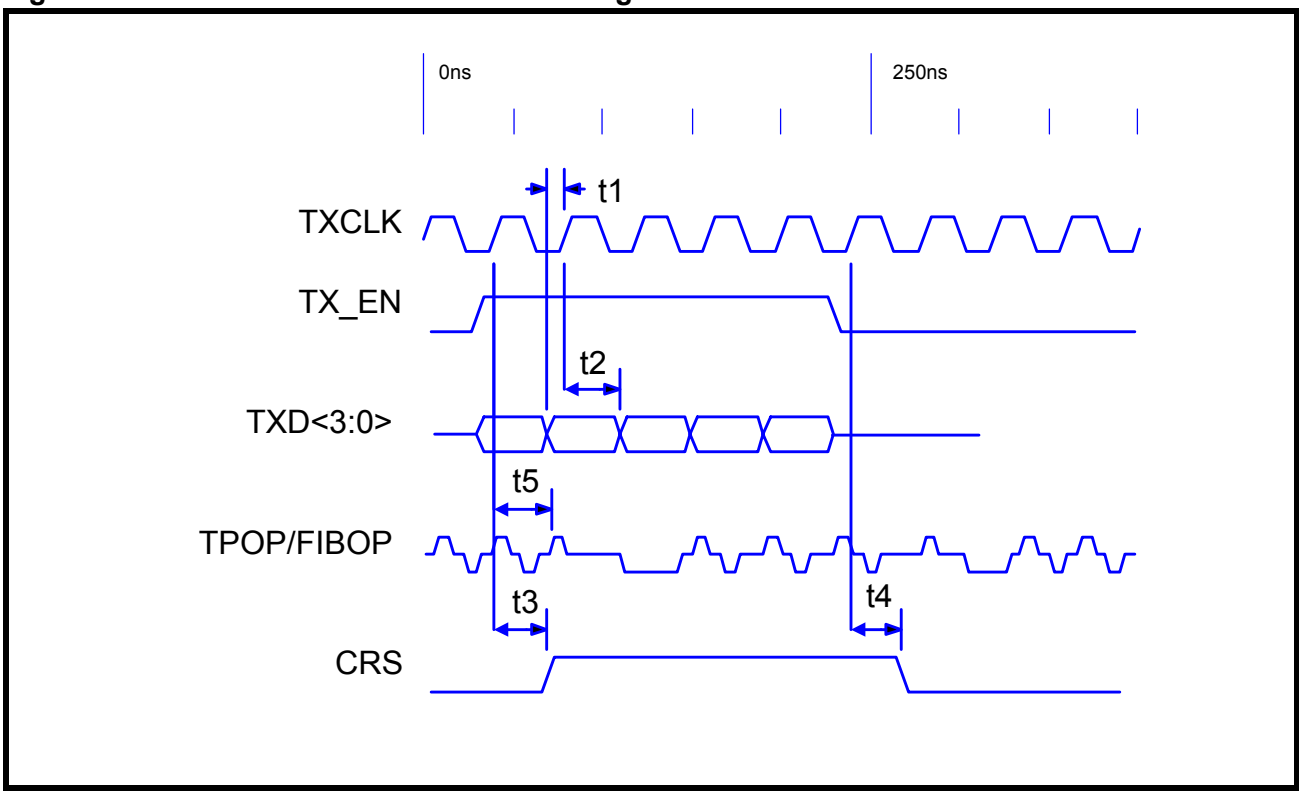


Table 30: MII - 100BASE-TX Transmit Timing Parameters / 4B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
TXD<3:0>, TX_EN, TX_ER Setup to TX_CLK High	t1	10	–	–	ns
TXD<3:0>, TX_EN, TX_ER Hold from TX_CLK High	t2	5	–	–	ns
TX_EN sampled to CRS asserted	t3	–	3	4	BT
TX_EN sampled to CRS de-asserted	t4	–	4	16	BT
TX_EN sampled to TPO out (Tx latency)	t5	6	10	14	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 18: MII - 100BASE-TX Receive Timing / 5B Mode

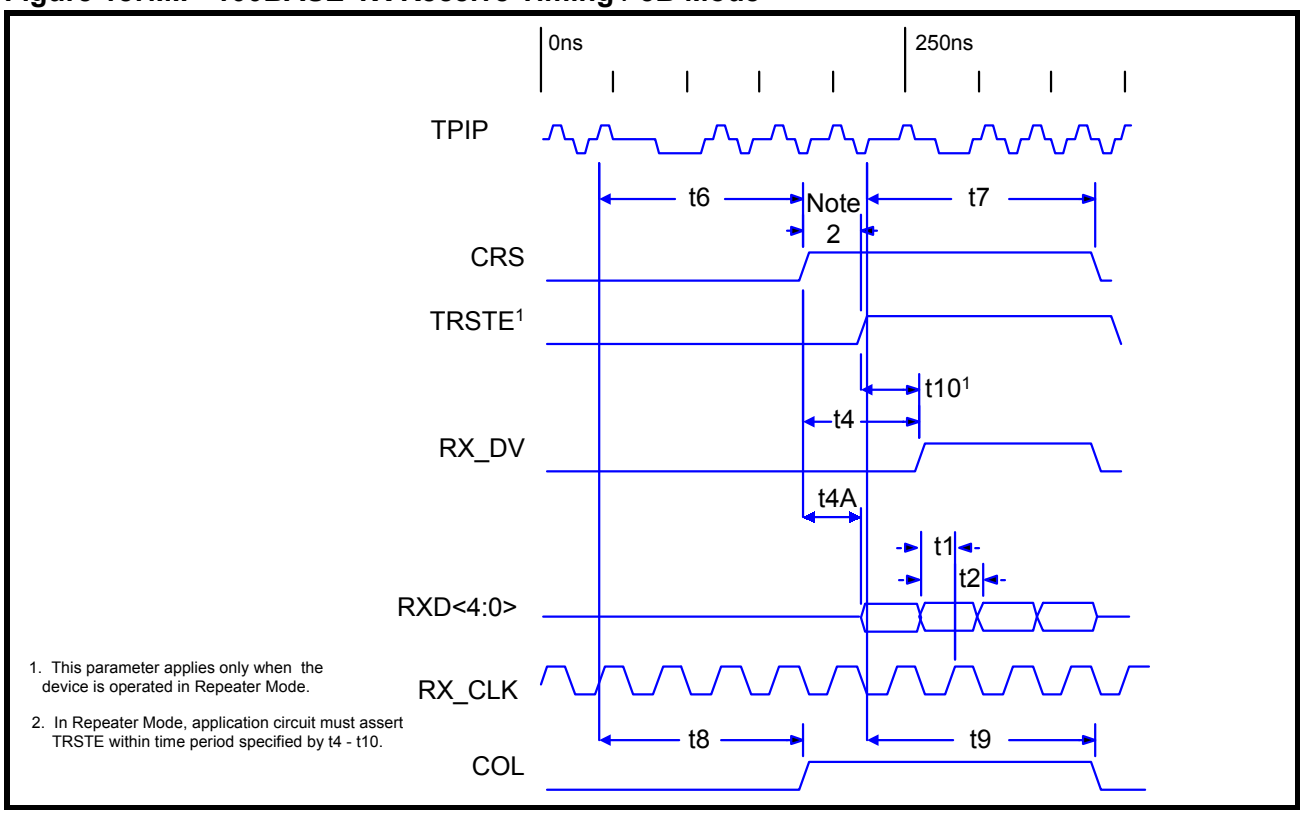


Table 31: MII - 100BASE-TX Receive Timing Parameters / 5B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	10	–	–	ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	5	–	–	ns
CRS asserted to RX_DV asserted	t4	–	8	–	BT
CRS asserted to RXD<4:0> asserted	t4A	–	4	–	BT
Receive start of "J" to CRS asserted	t6	0	15 - 19	20	BT
Receive start of "T" to CRS de-asserted	t7	13	23 - 27	28	BT
Receive start of "J" to COL asserted	t8	0	15 - 19	20	BT
Receive start of "T" to COL de-asserted	t9	13	23 - 27	28	BT
TRSTE asserted to RX_DV, RXD<4:0> driven[2]	t10	–	20	–	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. These parameters apply only when the device is operated in Repeater Mode

Figure 19: MII - 100BASE-TX Transmit Timing / 5B Mode

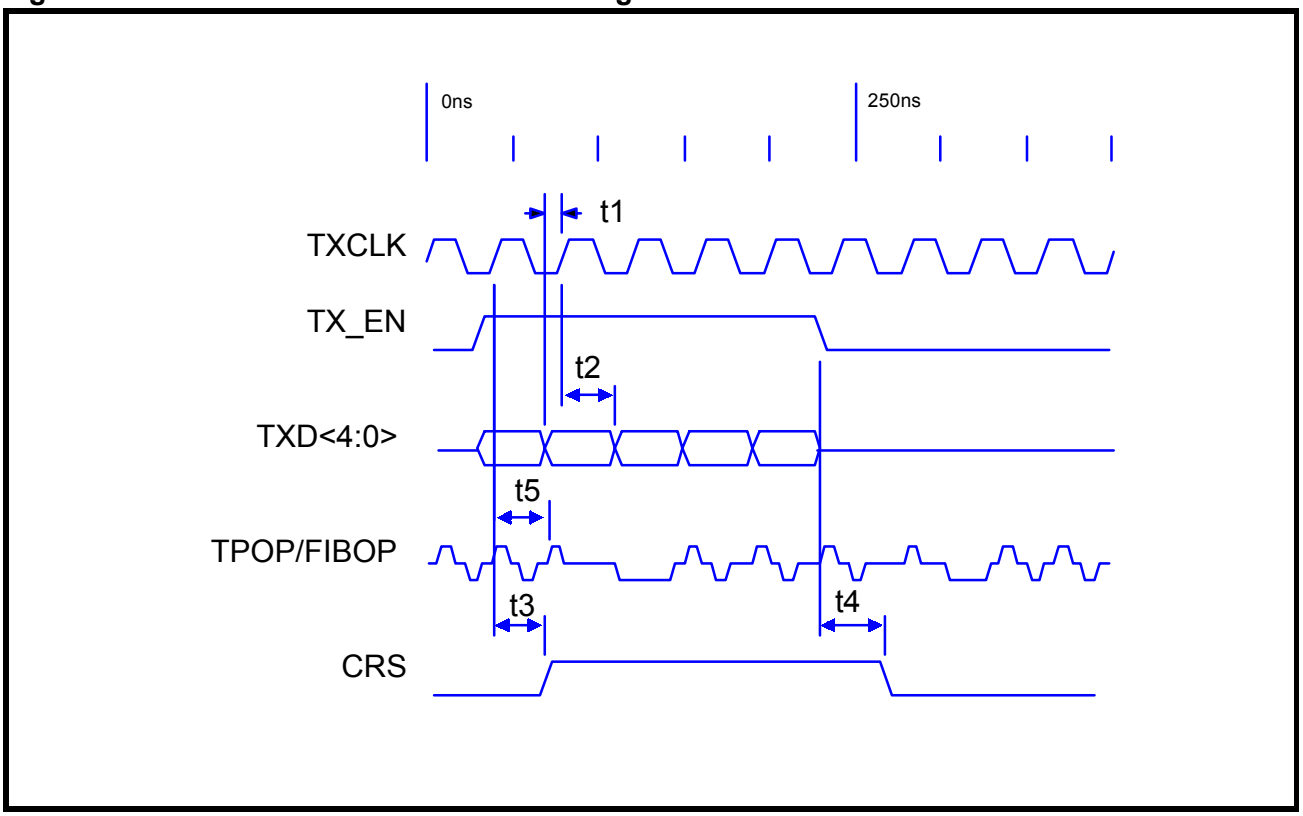


Table 32: MII - 100BASE-TX Transmit Timing Parameters / 5B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
TXD, TX_EN, TX_ER Setup to TX_CLK High	t1	10	–	–	ns
TXD, TX_EN, TX_ER Hold from TX_CLK High	t2	5	–	–	ns
TX_EN sampled to CRS asserted	t3	–	3	4	BT
TX_EN sampled to CRS de-asserted	t4	–	4	16	BT
TX_EN sampled to TPO out (Tx latency)	t5	4	6	9	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 20: MII - 100BASE-FX Receive Timing / 4B Mode

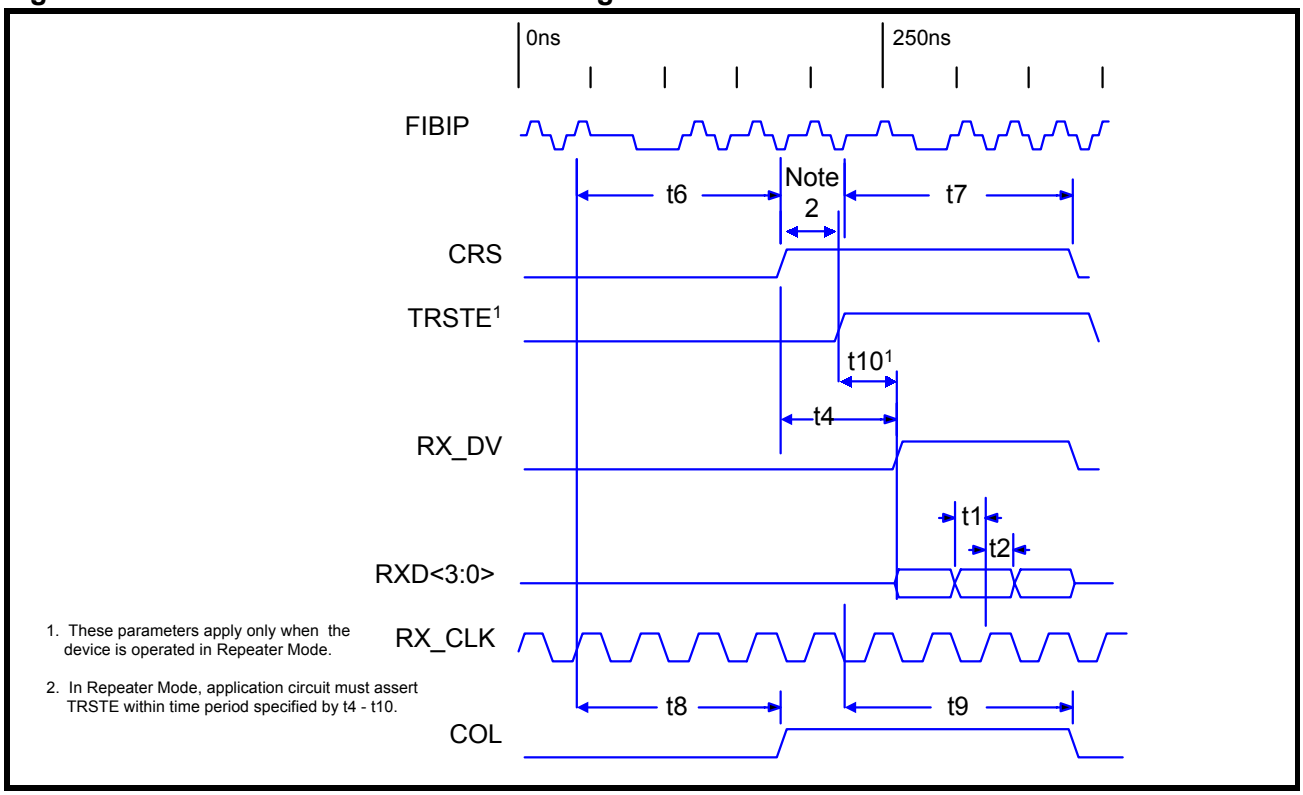


Table 33: MII - 100BASE-FX Receive Timing Parameters / 4B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	10	–	–	ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	5	–	–	ns
CRS asserted to RXD<3:0>, RX_DV asserted	t4	–	8	–	BT
Receive start of "J" to CRS asserted	t6	0	13 - 17	20	BT
Receive start of "T" to CRS de-asserted	t7	13	21 - 25	26	BT
Receive start of "J" to COL asserted	t8	0	13 - 17	20	BT
Receive start of "T" to COL de-asserted	t9	13	21 - 25	26	BT
TRSTE asserted to RX_DV, RXD<3:0> driven[2]	t10	–	20	–	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. These parameters apply only when the device is operated in Repeater Mode.

Figure 21: MII - 100BASE-FX Transmit Timing / 4B Mode

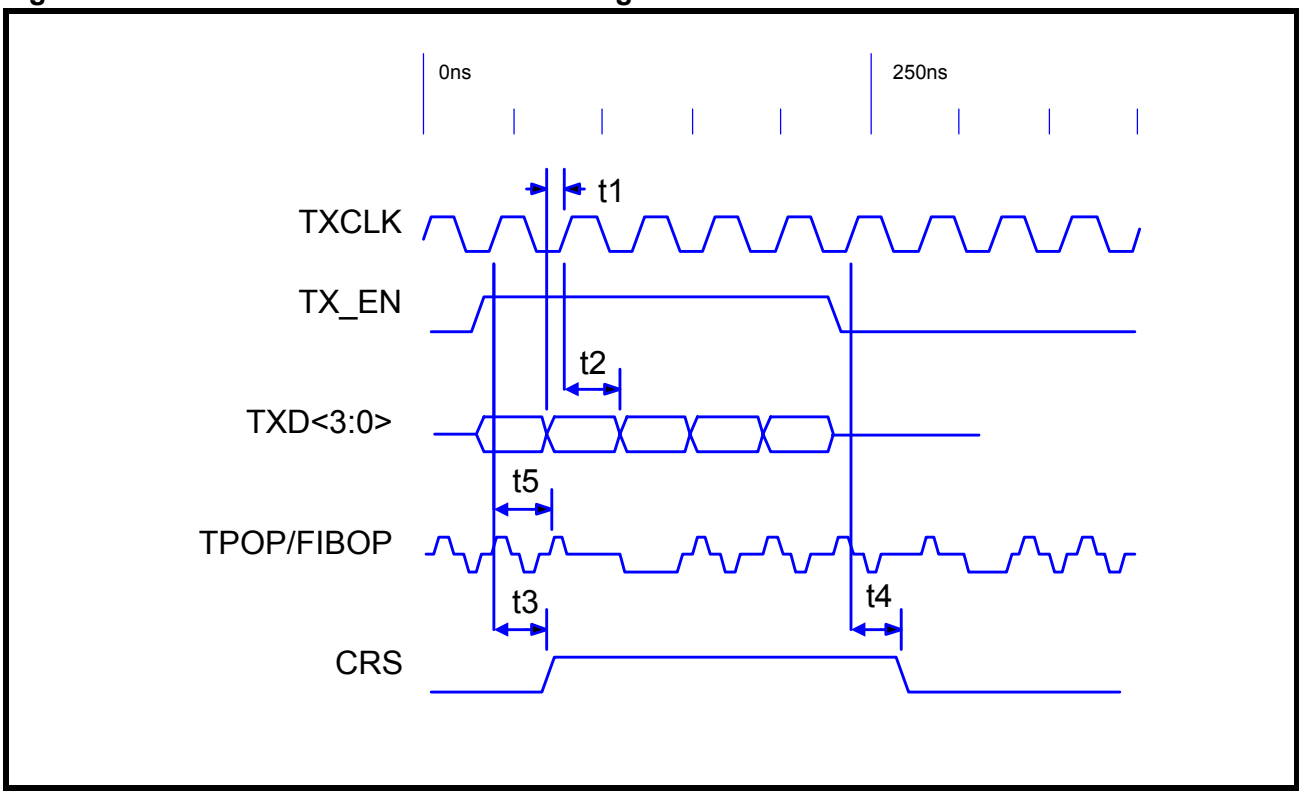


Table 34: MII - 100BASE-FX Transmit Timing Parameters / 4B Mode (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
TXD<3:0>, TX_EN, TX_ER Setup to TX_CLK High	t1	10	–	–	ns
TXD<3:0>, TX_EN, TX_ER Hold from TX_CLK High	t2	5	–	–	ns
TX_EN sampled to CRS asserted	t3	–	3	4	BT
TX_EN sampled to CRS de-asserted	t4	–	4	16	BT
TX_EN sampled to TPO out (Tx latency)	t5	6	11	14	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 22: MII - 10BASE-T Receive Timing

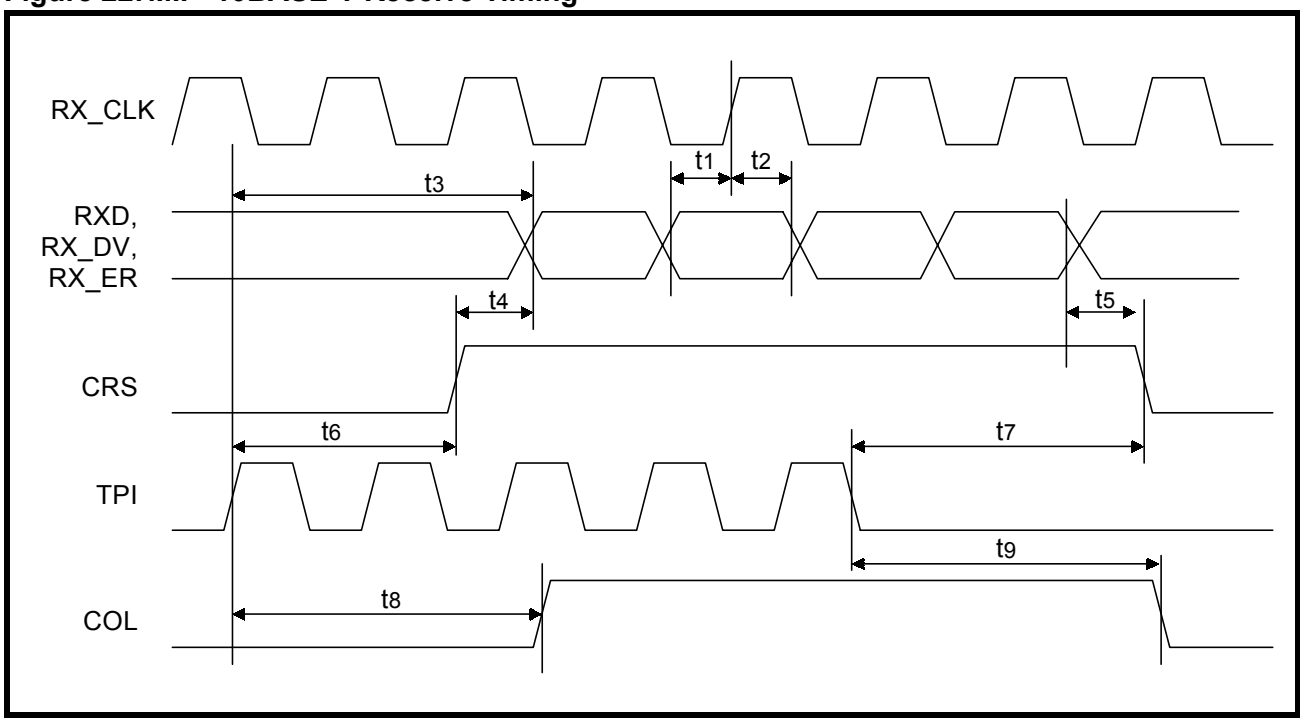


Table 35: MII - 10BASE-T Receive Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
RXD, RX_DV, RX_ER Setup to RX_CLK High	t1	10	–	–	ns
RXD, RX_DV, RX_ER Hold from RX_CLK High	t2	10	–	–	ns
TPI in to RXD out (Rx latency)	t3	–	–	73[3]	BT[2]
CRS asserted to RXD, RX_DV, RX_ER asserted	t4	0	–	69[3]	BT
RXD, RX_DV, RX_ER de-asserted to CRS de-asserted	t5	0	2.5 - 5.5	6	BT
TPI in to CRS asserted	t6	0	4	5	BT
TPI quiet to CRS de-asserted	t7	0	18	19	BT
TPI in to COL asserted	t8	0	4	5	BT
TPI quiet to COL de-asserted	t9	0	18	19	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. IEEE 802.3 defines BT as “the duration of one bit as transferred to and from the MAC. The bit time is the reciprocal of the bit rate. For example, for 10BASE-T the bit time is 10^{-7} or 100 ns.”
3. CRS is asserted. RXD/RX_DV are not driven during preamble and SFD (64 BT)

Figure 23: MII - 10BASE-T Transmit Timing

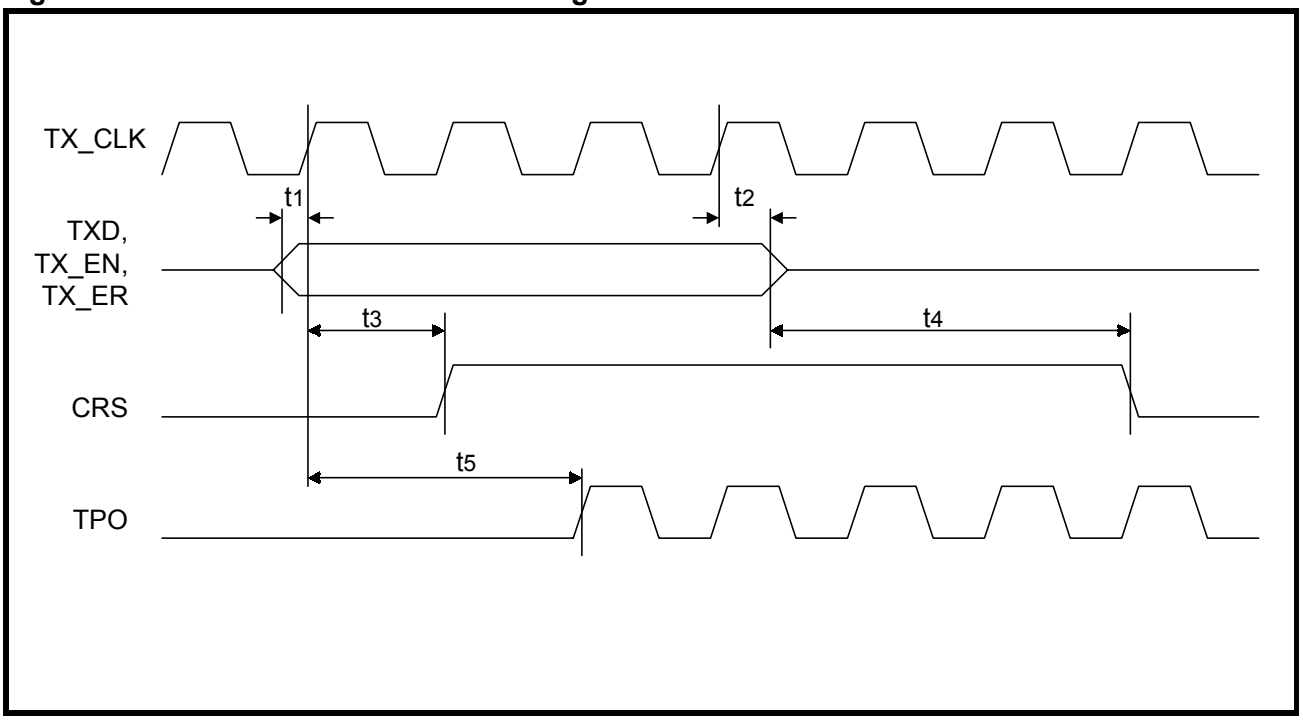


Table 36: MII - 10BASE-T Transmit Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units
TXD, TX_EN, TX_ER Setup to TX_CLK High	t1	10	–	–	ns
TXD, TX_EN, TX_ER Hold from TX_CLK High	t2	5	–	–	ns
TX_EN sampled to CRS asserted	t3	–	0	4	BT
TX_EN sampled to CRS de-asserted	t4	–	8	–	BT
TX_EN sampled to TPO out (Tx latency)	t5	–	3 - 5	–	BT

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 24: 10BASE-T SQE (Heartbeat) Timing

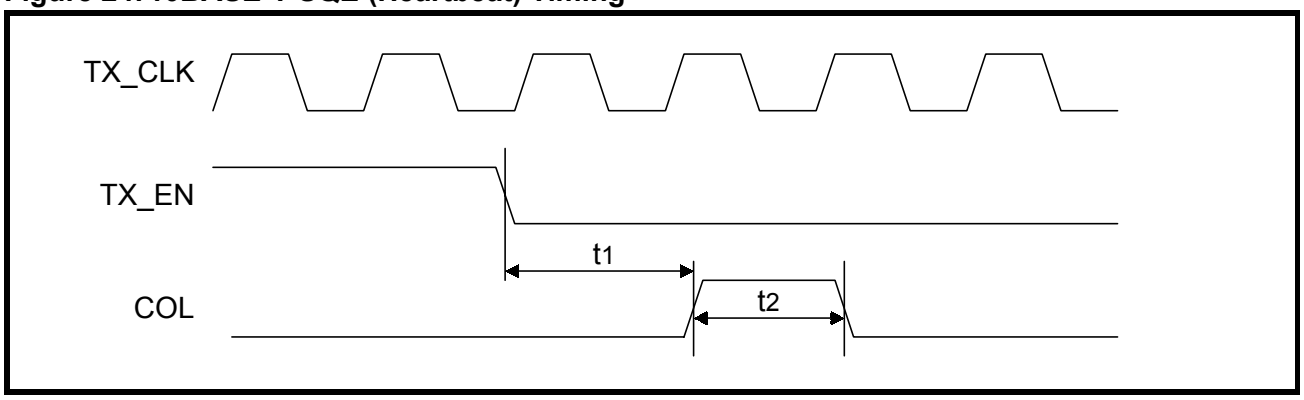


Table 37: 10BASE-T SQE (Heartbeat) Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
COL (SQE) Delay after TX_EN off	t1	0.65	1.0	1.6	µs	
COL (SQE) Pulse duration	t2	.5	1.0	1.5	µs	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 25: 10BASE-T Jab and Unjab Timing

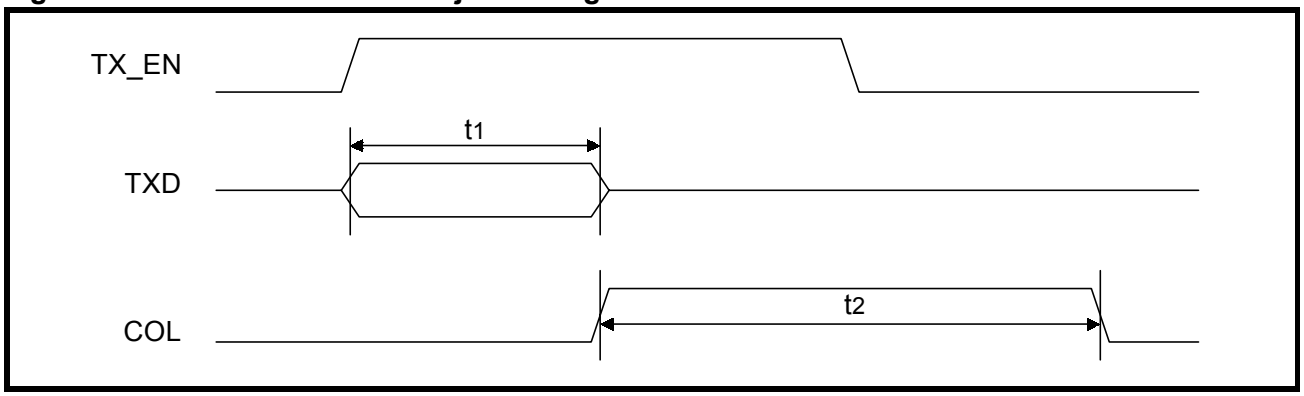


Table 38: 10BASE-T Jab and Unjab Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Maximum Transmit time	t1	20	96 - 128	150	ms	
Unjab time	t2	250	525	750	ms	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
Typical transmit and unjab times may be either of these values depending on internal 32 ms clock synchronization.

Figure 26: Auto Negotiation and Fast Link Pulse Timing

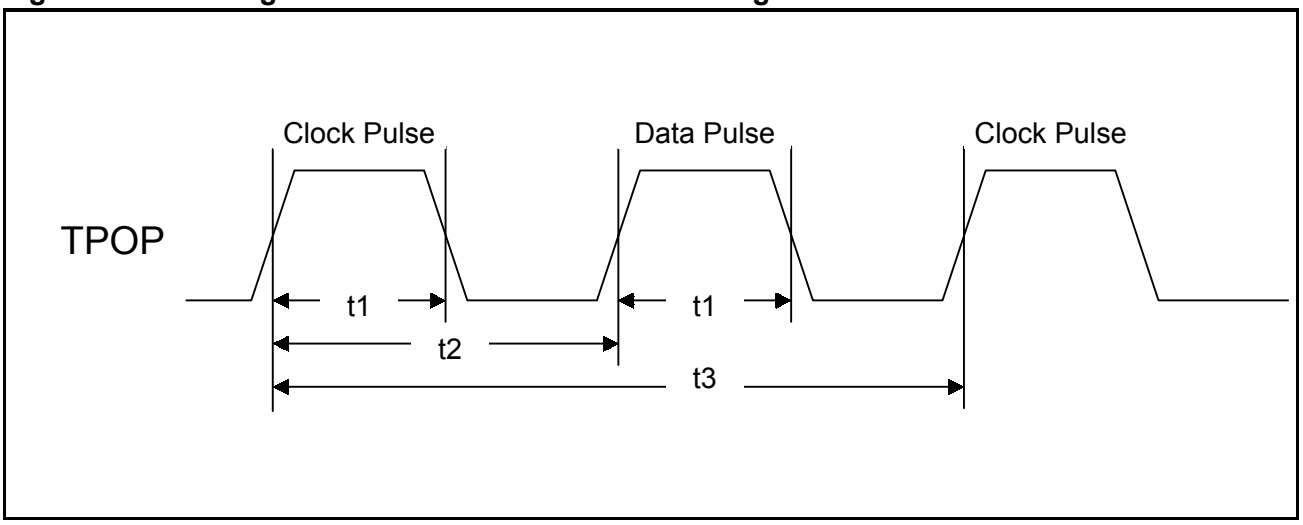


Figure 27: Fast Link Pulse Timing

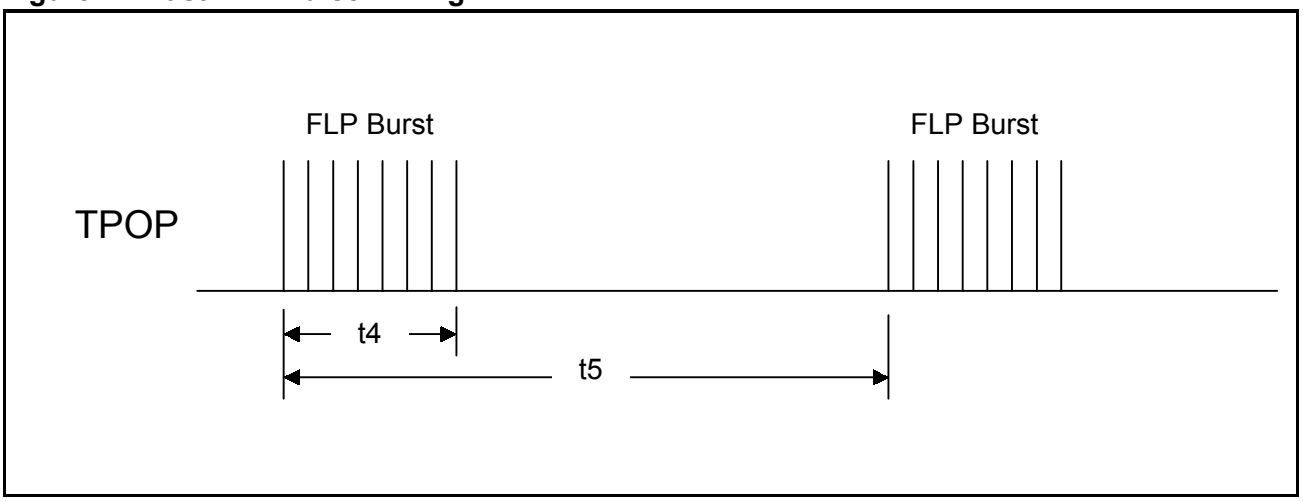


Table 39: Auto Negotiation and Fast Link Pulse Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Clock/Data pulse width	t1	–	100	–	ns	
Clock pulse to Data pulse	t2	55.5	62.5	69.5	µs	
Clock pulse to Clock pulse	t3	111	125	139	µs	
FLP burst width	t4	–	2	–	ms	
FLP burst to FLP burst	t5	8	12	24	ms	
Clock/Data pulses per burst	–	17	–	33	ea	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 28: MDIO Timing when Sourced by STA

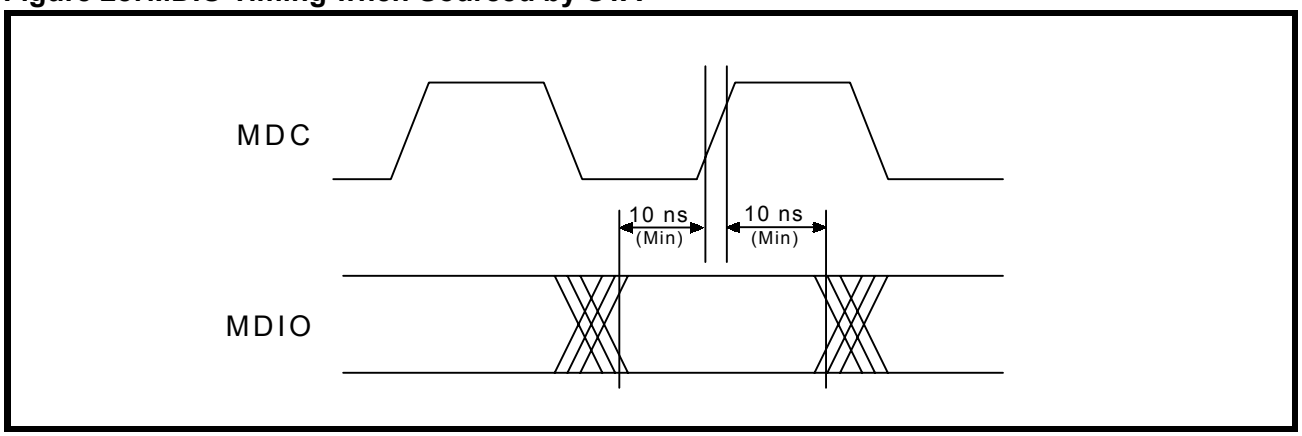


Figure 29: MDIO Timing when Sourced by PHY

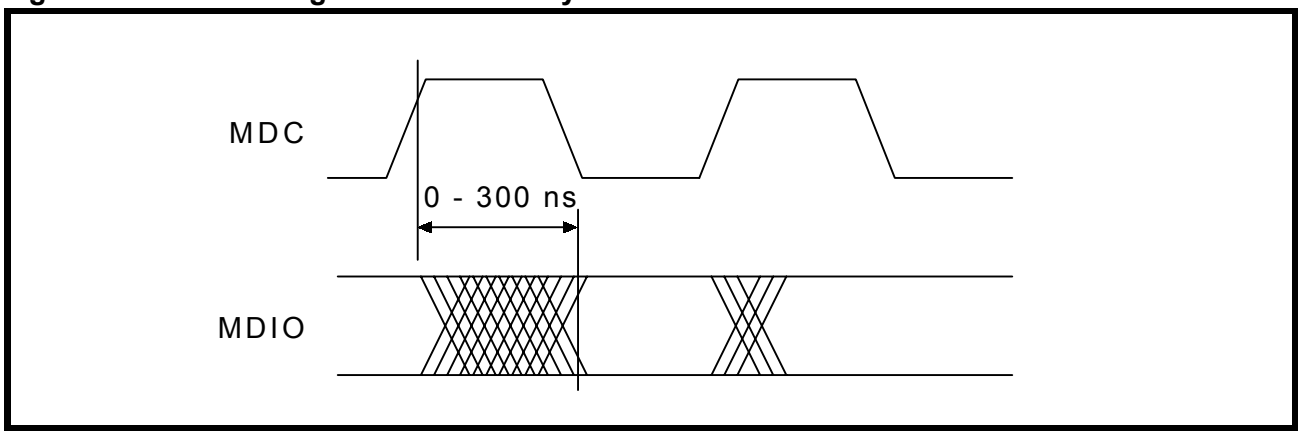


Table 40: MDIO Timing Parameters (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
MDIO Setup before MDC	–	10	–	–	ns	When sourced by STA
MDIO Hold after MDC	–	10	–	–	ns	When sourced by STA
MDC to MDIO Output delay	–	0	10	300	ns	When sourced by PHY

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 30: Miscellaneous Timing Parameters (Over Recommended Range)

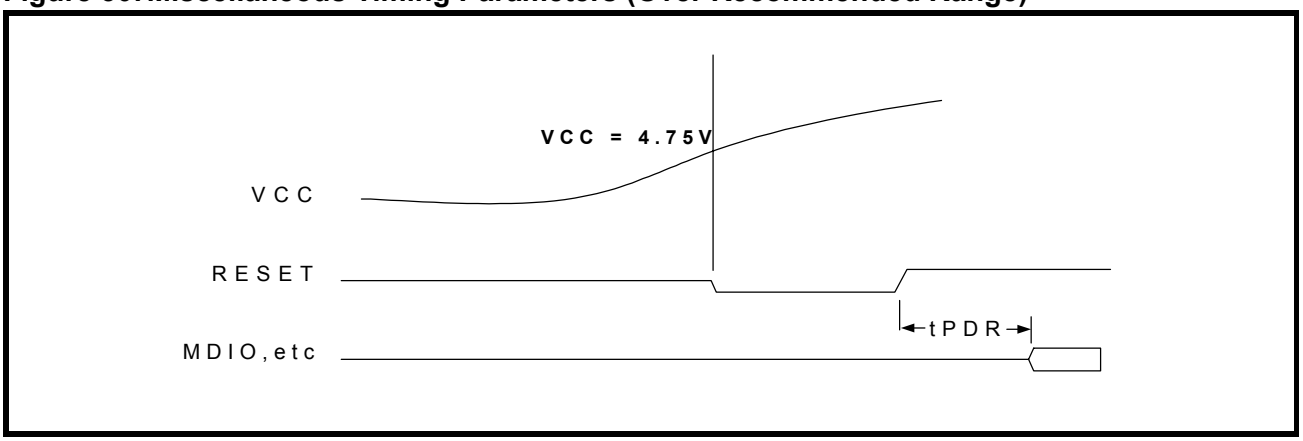


Table 41: Miscellaneous Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Power Down recovery time	t_{PDR}	–	50	–	ms	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

REGISTER DEFINITIONS

The LXT970 register set includes a total of 12 16-bit registers. Refer to Table 42 for a complete register listing.

- Seven base registers (0 through 6) are defined in accordance with the "Reconciliation Sublayer and Media Independent Interface" and "Physical Layer Link Signalling for 10/100 Mbps Auto-Negotiation" sections of the IEEE 802.3 specification (Register 7, Next Page, is not supported).
- Five additional registers (16 through 20) are defined in accordance with the IEEE 802.3 specification for adding unique chip functions.

Table 42: Register Set

Address	Register Name	Bit Assignments
0	Control Register	Refer to Table 43
1	Status Register	Refer to Table 44
2	PHY Identification Register 1	Refer to Table 45
3	PHY Identification Register 2	Refer to Table 46
4	Auto-Negotiation Advertisement Register	Refer to Table 47
5	Auto-Negotiation Link Partner Ability Register	Refer to Table 48
6	Auto-Negotiation Expansion Register	Refer to Table 49
16	Mirror Register	Refer to Table 50
17	Interrupt Enable Register	Refer to Table 51
18	Interrupt Status Register	Refer to Table 52
19	Configuration Register	Refer to Table 53
20	Chip Status Register	Refer to Table 54

Table 43: Control Register (Address 0)

Bit	Name	Description	Type [1]	Default
0.15	Reset	1 = Reset chip. 0 = Enable normal operation.	R/W SC	0
0.14	Loopback	1 = Enable loopback mode. When Loopback is enabled, during 100Mbps operation, the LXT970 disconnects its transmitter and receiver from the network. Data sent by the controller passes through the chip and then gets looped back to the MII. During 10Mbps operation, data is looped directly back to the MII. 0 = Disable loopback mode.	R/W	0
0.13	Speed Selection	1 = 100 Mbps 0 = 10 Mbps	R/W	Note 2
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiate process (overrides speed select and duplex mode bits). 0 = Disable auto-negotiate process.	R/W	Note 3
0.11	Power Down	1 = Enable power down. 0 = Enable normal operation.	R/W	Note 4
0.10	Isolate	1 = Electrically isolate LXT970 from MII. 0 = Normal operation.	R/W	Note 5
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process. 0 = Normal operation.	R/W SC	Note 6
0.8	Duplex Mode	1 = Enable full duplex. 0 = Enable half duplex.	R/W	Note 7
0.7	Collision Test	1 = Enable COL signal test. Bit 0.14 must be enabled to use this bit. This bit is used in conjunction with bit 0.14 to test the COL output. 0 = Disable COL signal test.	R/W	0 Note 8
0.6:4	Transceiver Test Mode	Not Supported	RO	0
0.3	Master-Slave Enable	Not Supported	RO	0
0.2	Master-Slave Value	Not Supported	RO	0
0.1:0	Reserved		R/W	0

1. R/W = Read/Write
   SC = Self Clearing
2. If auto-negotiation is enabled, this bit is ignored. If auto-negotiation is disabled, the default value of bit 0.13 is determined by pin CFG0.
3. The default value of bit 0.12 is determined by pin MF0/AUTO-NEG.
4. The LXT970 will internally reset all registers to their default values upon exiting power down mode. A delay of 500 ns minimum is required from the time power down is cleared until any register can be written.
5. The default value of bit 0.10 is determined by pin TRSTE.
6. If auto-negotiation is enabled, the default value of bit 0.9 is determined by pin CFG0. If auto-negotiation is disabled, the default value of bit 0.9 = 0.
7. If auto-negotiation is enabled, this bit is ignored. If auto-negotiation is disabled, the default value of bit 0.8 is determined by pin FDE.
8. This bit is ignored unless loopback is enabled (0.14 = 1).

Table 44: Status Register (Address 1)

Bit	Name	Description	Type [1]	Default
1.15	100BASE-T4	Not Supported	RO	0
1.14	100BASE-X Full Duplex	1 = LXT970 able to perform full duplex 100BASE-X.	RO	1
1.13	100BASE-X Half Duplex	1 = LXT970 able to perform half duplex 100BASE-X	RO	1
1.12	10 Mb/s Full Duplex	1 = LXT970 able to operate at 10 Mb/s in full duplex mode	RO	1
1.11	10 Mb/s Half Duplex	1 = LXT970 able to operate at 10 Mb/s in half duplex mode	RO	1
1.10	100BASE-T2 Full Duplex	Not Supported	RO	0
1.9	100BASE-T2 Half Duplex	Not Supported	RO	0
1.8	Reserved	Ignore on read	RO	0
1.7	Master-Slave Configuration Fault	Not Supported	RO	0
1.6	MF Preamble Suppression	0 = LXT970 will not accept management frames with preamble suppressed.	RO	0
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process complete. 0 = Auto-negotiation process not complete.	RO	0
1.4	Remote Fault	1 = Remote fault condition detected. 0 = No remote fault condition detected.	RO/LH	0
1.3	Auto-Negotiation Ability	1 = LXT970 is able to perform auto-negotiation.	RO	1
1.2	Link Status	1 = Link is up. 0 = Link is down.	RO/LL	0
1.1	Jabber Detect (10BASE-T Only)	1 = Jabber condition detected. 0 = No jabber condition detected.	RO/LH	0
1.0	Extended Capability	1 = Extended register capabilities.	RO	1

1. RO = Read Only
LL = Latching Low (This bit remains Low until read, and then returns High).
LH = Latching High (This bit remains High until read, and then returns Low).

Table 45: PHY Identification Register 1 (Address 2)

Bit	Name	Description	Type [1]	Default
2.15:0	PHY ID Number	The PHY identifier composed of bits 3 through 18 of the OUI.	RO	7810 hex

1. RO = Read Only

Table 46: PHY Identification Register 2 (Address 3)

Bit	Name	Description	Type [1]	Default
3.15:10	PHY ID number	The PHY identifier composed of bits 19 through 24 of the OUI.	RO	000000 bin
3.9:4	Manufacturer's model number	6 bits containing manufacturer's part number.	RO	000000 bin
3.3:0	Manufacturer's revision number	4 bits containing manufacturer's revision number.	RO	0000 bin

1. RO = Read Only

Figure 31: PHY Identifier Bit Mapping

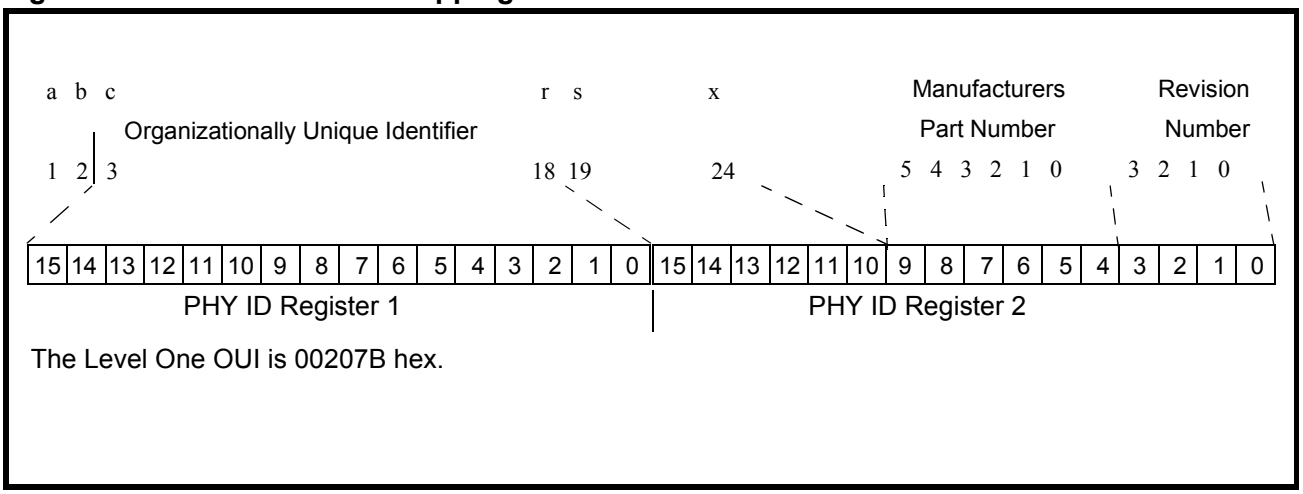


Table 47: Auto Negotiation Advertisement Register (Address 4)

Bit	Name	Description	Type [1]	Default
4.15	Next Page	Not Supported	RO	0
4.14	Reserved		RO	0
4.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	R/W	0
4.12:10	Reserved		R/W	0
4.9	100BASE-T4	1 = 100BASE-T4 capability is available. 0 = 100BASE-T4 capability is not available. (The LXT970 does not support 100BASE-T4 but allows this bit to be set to advertise in the Auto-Negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver could be switched in if this capability is desired.)	R/W	0
4.8	100BASE-TX Full Duplex	1 = DTE is 100BASE-TX full duplex capable. 0 = DTE is not 100BASE-TX full duplex capable.	R/W	Note 2
4.7	100BASE-TX	1 = DTE is 100BASE-TX capable. 0 = DTE is not 100BASE-TX capable.	R/W	Note 3
4.6	10BASE-T full duplex	1 = DTE is 10BASE-T full duplex capable. 0 = DTE is not 10BASE-T full duplex capable.	R/W	Note 4
4.5	10BASE-T	1 = DTE is 10BASE-T capable. 0 = DTE is not 10BASE-T capable.	R/W	Note 5
4.4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future Auto-Negotiation development <11111> = Reserved for future Auto-Negotiation development Unspecified or reserved combinations should not be transmitted.	R/W	00001

1. R/W = Read/Write
   RO = Read Only
2. The default value of bit 4.8 is determined by pin FDE ANDed with pin MF4/100BASE-TX/FX.
3. The default value of bit 4.7 is determined by pin MF4/100BASE-TX/FX.
4. The default value of bit 4.6 is determined by pin FDE AND'ed with pin CFG1.
5. The default value of bit 4.5 is determined by pin CFG1.

Table 48: Auto Negotiation Link Partner Ability Register (Address 5)

Bit	Name	Description	Type [1]	Default
5.15	Next Page	1 = Link Partner has ability to send multiple pages. 0 = Link Partner has no ability to send multiple pages.	RO	N/A
5.14	Acknowledge	1 = Link Partner has received Link Code Word from LXT970. 0 = Link Partner has not received Link Code Word from LXT970.	RO	N/A
5.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	RO	N/A
5.12:10	Reserved		RO	N/A
5.9	100BASE-T4	1 = Link Partner is 100BASE-T4 capable. 0 = Link Partner is not 100BASE-T4 capable.	RO	N/A
5.8	100BASE-TX full duplex	1 = Link Partner is 100BASE-TX full duplex capable. 0 = Link Partner is not 100BASE-TX full duplex capable.	RO	N/A
5.7	100BASE-TX	1 = Link Partner is 100BASE-TX capable. 0 = Link Partner is not 100BASE-TX capable.	RO	N/A
5.6	10BASE-T full duplex	1 = Link Partner is 10BASE-T full duplex capable. 0 = Link Partner is not 10BASE-T full duplex capable.	RO	N/A
5.5	10BASE-T	1 = Link Partner is 10BASE-T capable. 0 = Link Partner is not 10BASE-T capable.	RO	N/A
5.4:0	Selector Field S[4:0]	<00001> = IEEE 802.3 <00010> = IEEE 802.9 ISLAN-16T <00000> = Reserved for future Auto-Negotiation development <11111> = Reserved for future Auto-Negotiation development Unspecified or reserved combinations shall not be transmitted.	RO	N/A

1. RO = Read Only

Table 49: Auto Negotiation Expansion (Address 6)

Bit	Name	Description	Type [1]	Default
6.15:5	Reserved	Ignore.	RO	0
6.4	Parallel Detection Fault	1 = Parallel detection fault has occurred. 0 = Parallel detection fault has not occurred.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link partner is next page able. 0 = Link partner is not next page able.	RO	0

1. RO = Read Only
LH = Latching High (This bit remains High until read, and then returns Low).

Table 49: Auto Negotiation Expansion (Address 6) – continued

Bit	Name	Description	Type [1]	Default
6.2	Next Page Able	Not Supported	RO	0
6.1	Page Received	1 = 3 identical and consecutive link code words have been received from link partner. 0 = 3 identical and consecutive link code words have not been received from link partner.	RO/ LH	0
6.0	Link Partner Auto Neg Able	1 = Link partner is auto-negotiation able. 0 = Link partner is not auto-negotiation able.	RO	0

1. RO = Read Only
LH = Latching High (This bit remains High until read, and then returns Low).

Table 50: Mirror Register (Address 16, Hex 10)

Bit	Name	Description	Type [1]	Default
16.15:0	User Defined	This register is intended for use in checking the MII serial port and has no effect on chip operation.	R/W	0

1. R/W = Read /Write

Table 51: Interrupt Enable Register (Address 17, Hex 11)

Bit	Name	Description	Type [1]	Default
17.15:2	Reserved	Write as 0; ignore on read.	R/W	N/A
17.1	INTEN	1 = Enable interrupts on pin 2. Must be enabled for bit 17.0 or 19.12 to be effective. 0 = Enable Half/Full duplex indications on pin 2.	R/W	0
17.0	TINT	1 = Forces MDINT Low and sets bit 18.15 = 1. Also forces interrupt pulse on MDIO when bit 19.12 = 1. 0 = Normal operation. This bit is ignored unless the interrupt function is enabled (17.1 = 1).	R/W	0

1. R/W = Read /Write

Table 52: Interrupt Status Register (Address 18, Hex 12)

Bit	Name	Description	Type [1]	Default
18.15	MINT	1 = Indicates MII interrupt pending. 0 = Indicates no MII interrupt pending. This bit is cleared by reading Register 1 followed by reading Register 18.	RO	N/A
18.14	XTALOK	1 = Indicates that the LXT970 is fully powered up and the on-chip clocks are stable. 0 = Indicates that XTAL circuit is not stable.	RO	0
18.13:0	Reserved	Ignore	RO	0

1. RO = Read Only

Table 53: Configuration Register (Address 19, Hex 13)

Bit	Name	Description	Type [1]	Default
19.15	Reserved	Write as 0; ignore on read.	R/W	N/A
19.14	Txmit Test (100BASE-TX)	1 = 100BASE-T transmit test enabled, LXT970 will transmit data regardless of link status. This function is the analog of the link test function (19.8) for 100BASE-TX. 0 = Normal operation.	R/W	0
19.13	Repeater Mode	1 = Enable Repeater Mode. 0 = Enable DTE Mode.	R/W	Note 2
19.12	MDIO_INT	1 = Enable interrupt signaling on MDIO (if 17.1 = 1). 0 = Normal operation (MDIO Interrupt disabled). Bit is ignored unless the interrupt function is enabled (17.1 = 1).	R/W	0
19.11	TP Loopback (10BASE-T)	1 = Disable 10BT TP Loopback. Data transmitted by the MAC will not loopback to the RXD and RX_DV pins. CRS is asserted during a transmission only in DTE mode and half-duplex operation. 0 = Enable 10BT TP Loopback	R/W	0
19.10	SQE (10BASE-T)	1 = Enable SQE. 0 = Disable SQE (Default).	R/W	0
19.9	Jabber (10BASE-T)	1 = Disable jabber. 0 = Normal operation (jabber enabled).	R/W	0
19.8	Link Test (10BASE-T)	1 = Disable 10BASE-T link integrity test. 0 = Normal operation (10BASE-T link integrity test enabled).	R/W	Note 3

1. R/W = Read/Write
2. The default value of bit 19.13 is determined by pin MF1/AUTO-NEG.
3. If auto-negotiation is disabled, the default value of bit 19.8 is determined by pin CFG1. If auto-neg is enabled, the default value of bit 19.8 = 0.
4. The default value of bit 19.4 is determined by pin MF2/ENCODER Operation.
5. The default value of bit 19.3 is determined by pin MF3/SCRAMBLER Operation.
6. If auto-negotiation is disabled, default value of bit 19.2 is determined by pin MF4/100BASE-TX/FX. If auto-negotiation is enabled, default value of bit 19.2 = 0.

Table 53: Configuration Register (Address 19, Hex 13) – continued

Bit	Name	Description	Type [1]	Default
19.7:6	LEDC Programming bits	Determine condition indicated by LEDC. bit 7 bit 6 Description 0 0 LEDC indicates collision 0 1 LEDC is off 1 0 LEDC indicates activity. 1 1 LEDC is continuously on (for diagnostic use).	R/W	0,0
19.5	Advance TX Clock	1 = TX clock is advanced relative to TXD<4:0> and TX_ER by 1/2 TX_CLK cycle. 0 = Normal operation.	R/W	0
19.4	4B Nibble/ 5BSymbol (100BASE-X only)	1 = 5-bit Symbol Mode (Bypass encoder/decoder); RXD<4:0> symbol data is not aligned. 0 = 4-bit Nibble Mode (Normal operation).	R/W	Note 4
19.3	Scrambler (100BASE-X only)	1 = Bypass transmit scrambler and receive descrambler. 0 = Normal operation (scrambler and descrambler enabled). In FX mode, the LXT970 *automatically* bypasses the Scrambler. *Selecting* Scrambler bypass in FX mode will cause the LXT970 to also bypass the 4B/5B encoder and enable Symbol mode MII operation.	R/W	Note 5
19.2	100BASE-FX	1 = Enable 100BASE fiber interface. 0 = Enable 100BASE twisted pair interface.	R/W	Note 6
19.1	Reserved	Write as 0; Ignore on read.	R/W	0
19.0	Transmit Disconnect	1 = Disconnect TP transmitter from line. 0 = Normal operation.	R/W	0

1. R/W = Read/Write
2. The default value of bit 19.13 is determined by pin MF1/AUTO-NEG.
3. If auto-negotiation is disabled, the default value of bit 19.8 is determined by pin CFG1. If auto-neg is enabled, the default value of bit 19.8 = 0.
4. The default value of bit 19.4 is determined by pin MF2/ENCODER Operation.
5. The default value of bit 19.3 is determined by pin MF3/SCRAMBLER Operation.
6. If auto-negotiation is disabled, default value of bit 19.2 is determined by pin MF4/100BASE-TX/FX. If auto-negotiation is enabled, default value of bit 19.2 = 0.

Table 54: Chip Status Register (Address 20, Hex 14)

Bit	Name	Description	Type [1]	Default
20.15:14	Reserved	Ignore.	RO	N/A
20.13	Link	1 = Link is up. 0 = Link is down. Link bit 20.13 is a duplicate of bit 1.2, except that it is a dynamic indication, whereas bit 1.2 latches Low.	RO	0
20.12	Duplex Mode	1 = Full Duplex. 0 = Half Duplex.	RO	Note 2
20.11	Speed	1 = 100 Mbps operation. 0 = 10 Mbps operation.	RO	Note 2
20.10	Reserved	Ignore.	RO	N/A
20.9	Auto-Negotiation Complete	1 = Auto-negotiation process complete. 0 = Auto-negotiation process not complete. Auto-Negotiation Complete bit 20.9 is a duplicate of bit 1.5.	RO/LH	0
20.8	Page Received	1 = Three identical and consecutive link code words have been received. 0 = Three identical and consecutive link code words have not been received. Page Received bit 20.8 is a duplicate of bit 6.1	RO/LH	0
20:7	Reserved	Write as 0; Ignore on read.	RO/LH	0
20.6	Stream scrambler/ decoder lock (100BASE-TX only)	1 = Stream scrambler/decoder locked. 0 = Stream scrambler/decoder not locked.	RO	0
20.5	Symbol Error	1 = Symbol error detected. 0 = No symbol error detected.	RO/LH	N/A
20.4	MLT3 Encoding Error	1 = MLT3 encoding error detected. 0 = No MLT3 encoding error detected.	RO/LH	N/A
20.3	Reserved	Ignore.	RO	N/A
20.2	Low Voltage	1 = Low voltage fault on VCC has occurred. 0 = No fault.	RO/LH	N/A
20.1	Reserved	Ignore.	RO	N/A
20.0	PLL Lock (100BASE-TX)	1 = 100BASE-TX/FX Receiver PLL is not locked. 0 = PLL is locked.	RO/LH	N/A

1. RO = Read Only
   LH = Latching High (This bit remains High until read, and then returns Low).
2. Bits 20.12 and 20.11 reflect the current operating mode of the LXT970.

NOTES