

### FEATURES

- All switches off with power supply off
- Analog output of on channel clamped within power supplies if an overvoltage occurs
- Latch-up proof construction
- Low on resistance (270  $\Omega$  typical)
- Fast switching times
  - $t_{ON}$ : 230 ns maximum
  - $t_{OFF}$ : 130 ns maximum
- Low power dissipation (3.3 mW maximum)
- Fault and overvoltage protection ( $-40$  V to  $+55$  V)
- Break-before-make construction
- TTL and CMOS compatible inputs

### APPLICATIONS

- Existing multiplexer applications (both fault-protected and nonfault-protected)
- New designs requiring multiplexer functions

### GENERAL DESCRIPTION

The [ADG508F](#) and [ADG509F](#) are CMOS analog multiplexers, with the [ADG508F](#) comprising eight single channels and the [ADG509F](#) comprising four differential channels. These multiplexers provide fault protection. Using a series n-channel, p-channel, n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs from  $-40$  V to  $+55$  V. During fault conditions with power supplies off, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources that drive the multiplexer.

The [ADG508F](#) switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1, and A2. The [ADG509F](#) switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched off.

### FUNCTIONAL BLOCK DIAGRAMS

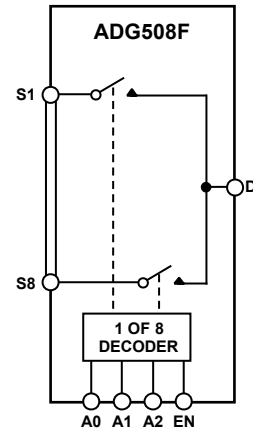


Figure 1.

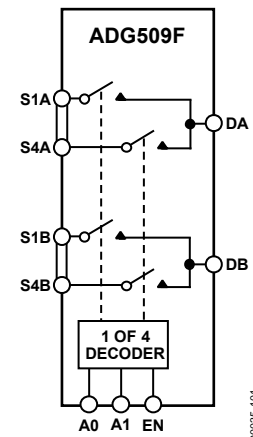


Figure 2.

### PRODUCT HIGHLIGHTS

1. Fault protection. The [ADG508F/ADG509F](#) can withstand continuous voltage inputs from  $-40$  V to  $+55$  V. When a fault occurs due to the power supplies being turned off, all the channels are turned off and only a leakage current of a few nanoamperes flows.
2. On channel saturates while fault exists.
3. Low  $R_{ON}$ .
4. Fast switching times.
5. Break-before-make switching. Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Trench isolation eliminates latch-up. A dielectric trench separates the p and n-channel MOSFETs thereby preventing latch-up.

#### Rev. F

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## REVISION HISTORY

### 7/11—Rev. E to Rev. F

Deleted ADG528F .....	Universal
Changes to Features Section and General Description Section ..	1
Changes to Specifications Section .....	3
Deleted Timing Diagrams Section .....	4
Changes to Table 4.....	5
Added Table 5.....	6
Added Table 6.....	7
Replaced Typical Performance Characteristics Section .....	8
Changes to Terminology Section.....	10
Changes to Figure 27 and Figure 28.....	13
Changes to Figure 31 .....	14
Changes to Theory of Operation Section.....	11
Updated Outline Dimensions .....	15
Changes to Ordering Guide .....	17

### 7/09—Rev. D: Rev. E

Updated Format .....	Universal
Added TSSOP .....	Universal
Updated Outline Dimensions .....	15
Changes to Ordering Guide .....	18

### 4/01—Data Sheet Changed from Rev. C to Rev. D.

Changes to Ordering Guide .....	1
Changes to Specifications Table.....	2
Max Ratings Changed .....	4
Deleted 16-Lead Cerdip from Outline Dimensions .....	11
Deleted 18-Lead Cerdip from Outline Dimensions .....	12

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range	$V_{SS} + 1.4$ $V_{DD} - 1.4$		V typ V typ	Output open circuit
$R_{ON}$	$V_{SS} + 2.2$ $V_{DD} - 2.2$		V typ V typ	Output loaded, 1 mA
	270	350	$\Omega$ typ	$-10\text{ V} \leq V_S \leq +10\text{ V}$ , $I_S = 1\text{ mA}$ ; $V_{DD} = +15\text{ V} \pm 10\%$ , $V_{SS} = -15\text{ V} \pm 10\%$ See Figure 21
		390	$\Omega$ max	
$R_{ON}$ Drift	0.6		%/°C typ	$V_S = 0\text{ V}$ , $I_S = 1\text{ mA}$
On-Resistance Match Between Channels, $\Delta R_{ON}$	3		% max	$V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage $I_S$ (Off)	$\pm 0.02$		nA typ	$V_D = \pm 10\text{ V}$ , $V_S = \mp 10\text{ V}$ ; See Figure 22
Drain Off Leakage $I_D$ (Off)	$\pm 1$	$\pm 50$	nA max	
	$\pm 0.04$		nA typ	$V_D = \pm 10\text{ V}$ , $V_S = \mp 10\text{ V}$ ; See Figure 23
Channel On Leakage $I_D, I_S$ (On)	$\pm 1$	$\pm 60$	nA max	
	$\pm 1$	$\pm 30$	nA max	$V_S = V_D = \pm 10\text{ V}$ ; See Figure 24
ADG508F	$\pm 0.04$		nA typ	
	$\pm 1$	$\pm 60$	nA max	
ADG509F	$\pm 1$	$\pm 30$	nA max	
ADG508F	$\pm 0.04$		nA typ	
	$\pm 1$	$\pm 60$	nA max	
ADG509F	$\pm 1$	$\pm 30$	nA max	
<b>FAULT</b>				
Source Leakage Current $I_S$ (Fault) (With Overvoltage)	$\pm 0.02$		nA typ	$V_S = +55\text{ V}$ or $-40\text{ V}$ , $V_D = 0\text{ V}$ , see Figure 25
Drain Leakage Current $I_D$ (Fault) (With Overvoltage)	$\pm 2$	$\pm 2$	$\mu\text{A}$ max	
	$\pm 5$		nA typ	$V_S = \pm 25\text{ V}$ , $V_D = \mp 10\text{ V}$ , see Figure 23
Source Leakage Current $I_S$ (Fault) (Power Supplies Off)	$\pm 2$		$\mu\text{A}$ max	
	$\pm 1$		nA typ	$V_S = \pm 25\text{ V}$ , $V_D = V_{EN} = A0, A1, A2 = 0\text{ V}$ See Figure 26
$\pm 2$		$\mu\text{A}$ max		
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current, $I_{INL}$ OR $I_{INH}$		$\pm 1$	$\mu\text{A}$ max	$V_{IN} = 0$ or $V_{DD}$
$C_{IN}$ , Digital Input Capacitance	5		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>				
$t_{TRANSITION}$	175		ns typ	$R_L = 1\text{ M}\Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = \pm 10\text{ V}$ , $V_{S8} = \mp 10\text{ V}$ ; see Figure 27
	220	300	ns max	
$t_{OPEN}$	90		ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 5\text{ V}$ ; see Figure 28
	60	40	ns min	
$t_{ON}$ (EN)	180		ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 5\text{ V}$ ; see Figure 29
	230	300	ns max	
$t_{OFF}$ (EN)	100		ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$
	130	150	ns typ	
$t_{SETT}$ , Settling Time			ns max	$V_S = 5\text{ V}$ ; see Figure 29
	0.1%	1	$\mu\text{s}$ typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 5\text{ V}$
	0.01%	2.5	$\mu\text{s}$ typ	

# ADG508F/ADG509F

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
Charge Injection	15		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\ \text{nF}$ ; see Figure 30 $R_L = 1\ \text{k}\Omega$ , $C_L = 15\ \text{pF}$ , $f = 100\ \text{kHz}$ ; $V_S = 7\ \text{V rms}$ ; see Figure 31
Off Isolation	93		dB typ	
$C_S$ (Off)	3		pF typ	
$C_D$ (Off)				
ADG508F ADG509F	22 12		pF typ pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.05	0.2	mA max	$V_{IN} = 0\ \text{V or } 5\ \text{V}$
$I_{SS}$	0.1	1	$\mu\text{A max}$	

<sup>1</sup> Guaranteed by design, not subject to production test.

## TRUTH TABLES

Table 2. ADG508F Truth Table<sup>1</sup>

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

<sup>1</sup> X = don't care.

Table 3. ADG509F Truth Table<sup>1</sup>

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

<sup>1</sup> X = don't care.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise noted.

**Table 4.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	48 V
$V_{DD}$ to GND	-0.3 V to +48 V
$V_{SS}$ to GND	+0.3 V to -48 V
Digital Input, EN, Ax	-0.3 V to $V_{DD} + 0.3$ V or 20 mA, whichever occurs first
$V_S$ , Analog Input Overvoltage with Power On ( $V_{DD} = +15$ V, $V_{SS} = -15$ V)	$V_{SS} - 25$ V to $V_{DD} + 40$ V
$V_S$ , Analog Input Overvoltage with Power Off ( $V_{DD} = 0$ V, $V_{SS} = 0$ V)	-40 V to +55 V
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA
Operating Temperature Range Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
TSSOP	
$\theta_{JA}$ , Thermal Impedance Plastic DIP Package	112°C/W
$\theta_{JA}$ , Thermal Impedance 16-Lead	117°C/W
SOIC Package	
$\theta_{JA}$ , Thermal Impedance Narrow Body	77°C/W
Wide Body	75°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG508F/ADG509F

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

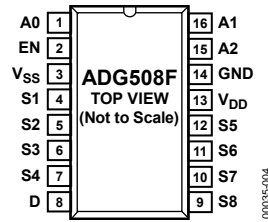


Figure 3. ADG508F Pin Configuration

Table 5. ADG508F Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V <sub>SS</sub>	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1	Source Terminal 1. This pin can be an input or an output.
5	S2	Source Terminal 2. This pin can be an input or an output.
6	S3	Source Terminal 3. This pin can be an input or an output.
7	S4	Source Terminal 4. This pin can be an input or an output.
8	D	Drain Terminal. This pin can be an input or an output.
9	S8	Source Terminal 8. This pin can be an input or an output.
10	S7	Source Terminal 7. This pin can be an input or an output.
11	S6	Source Terminal 6. This pin can be an input or an output.
12	S5	Source Terminal 5. This pin can be an input or an output.
13	V <sub>DD</sub>	Most Positive Power Supply Potential.
14	GND	Ground (0 V) Reference.
15	A2	Logic Control Input.
16	A1	Logic Control Input.

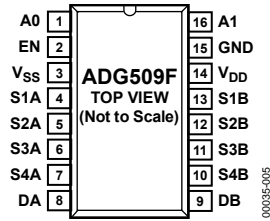


Figure 4. ADG509F Pin Configuration

Table 6. ADG509F Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V <sub>SS</sub>	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1A	Source Terminal 1A. This pin can be an input or an output.
5	S2A	Source Terminal 2A. This pin can be an input or an output.
6	S3A	Source Terminal 3A. This pin can be an input or an output.
7	S4A	Source Terminal 4A. This pin can be an input or an output.
8	DA	Drain Terminal A. This pin can be an input or an output.
9	DB	Drain Terminal B. This pin can be an input or an output.
10	S4B	Source Terminal 4B. This pin can be an input or an output.
11	S3B	Source Terminal 3B. This pin can be an input or an output.
12	S2B	Source Terminal 2B. This pin can be an input or an output.
13	S1B	Source Terminal 1B. This pin can be an input or an output.
14	V <sub>DD</sub>	Most Positive Power Supply Potential.
15	GND	Ground (0 V) Reference.
16	A1	Logic Control Input.

## TYPICAL PERFORMANCE CHARACTERISTICS

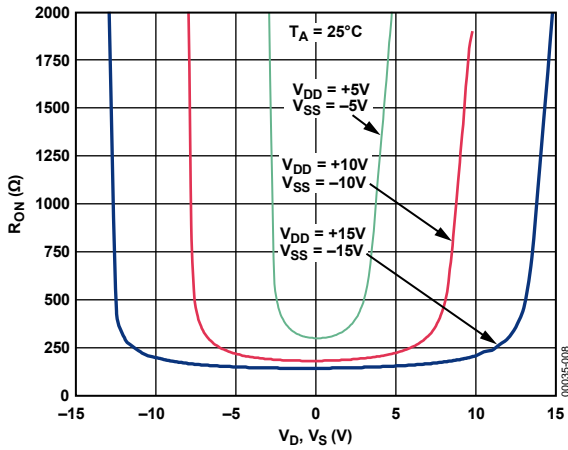


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ )

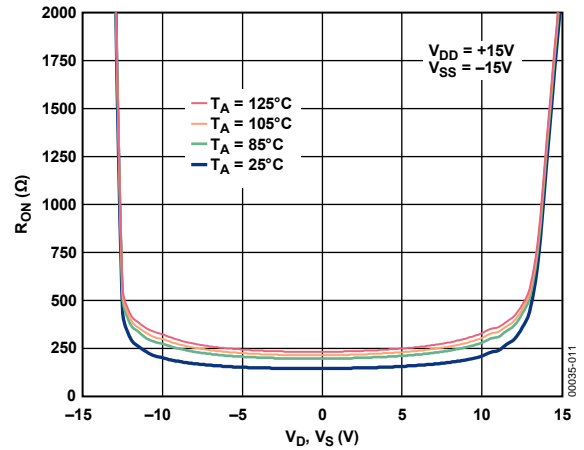


Figure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

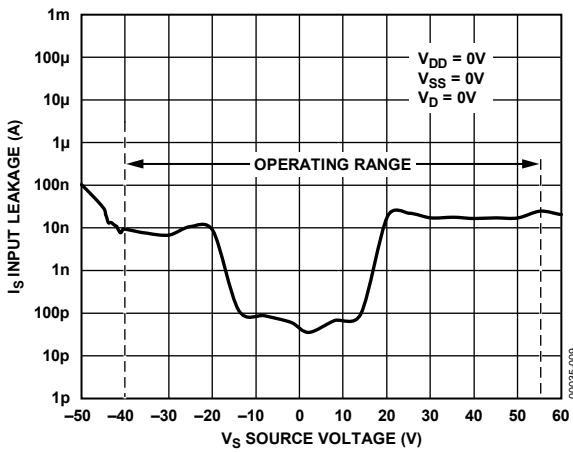


Figure 6. Source Input Leakage Current as a Function of  $V_S$  (Power Supplies Off) During Overvoltage Conditions

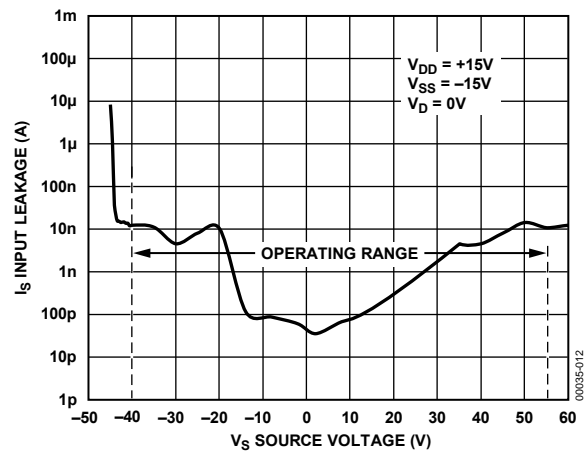


Figure 9. Source Input Leakage Current as a Function of  $V_S$  (Power Supplies On) During Overvoltage Conditions

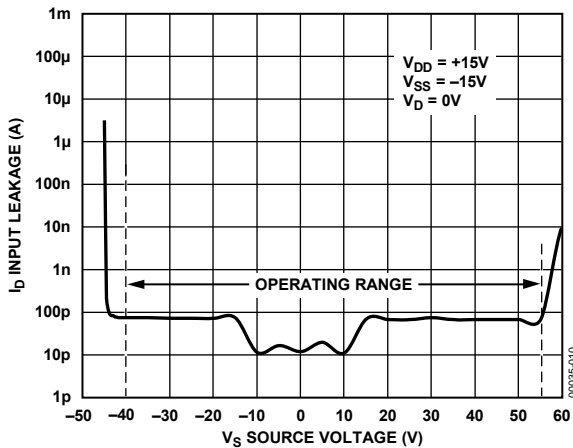


Figure 7. Drain Output Leakage Current as a Function of  $V_S$  (Power Supplies On) During Overvoltage Conditions

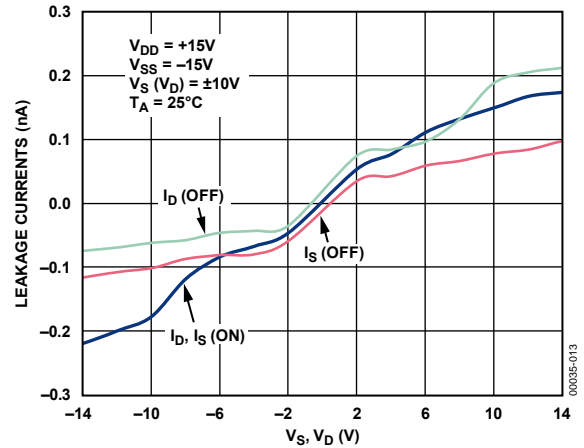


Figure 10. Leakage Currents as a Function of  $V_D$  ( $V_S$ )



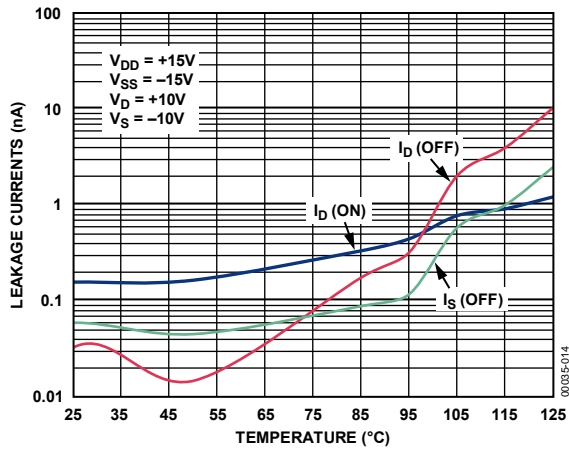


Figure 11. Leakage Currents as a Function of Temperature

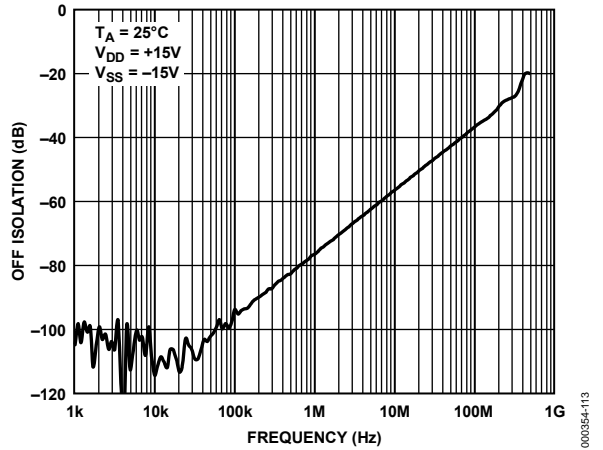


Figure 14. Off Isolation vs. Frequency,  $\pm 15 V$  Dual Supply

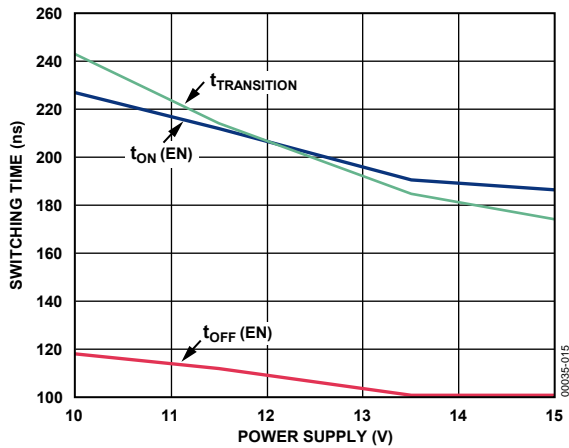


Figure 12. Switching Time vs. Dual Power Supply

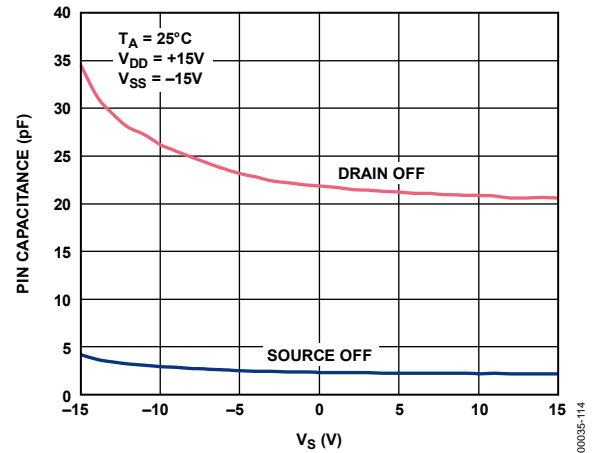


Figure 15. Capacitance vs. Source Voltage

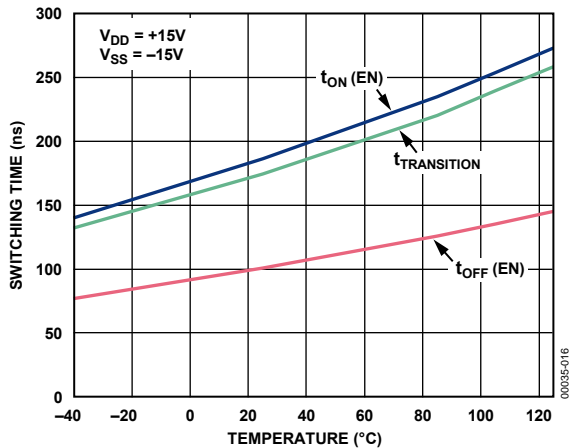


Figure 13. Switching Time vs. Temperature

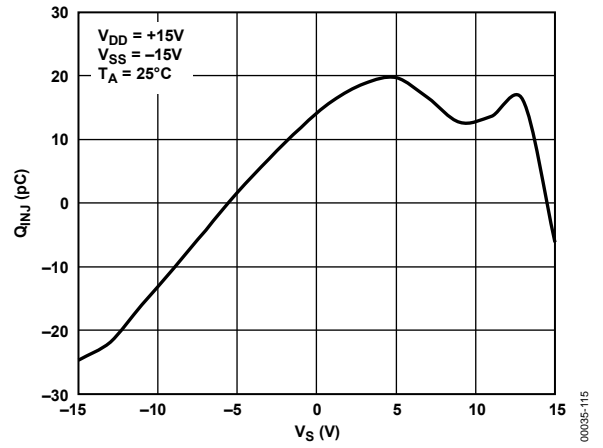


Figure 16. Charge Injection vs. Source Voltage

## TERMINOLOGY

<b>V<sub>DD</sub></b> Most positive power supply potential.	<b>C<sub>D</sub> (Off)</b> Channel output capacitance for off condition.
<b>V<sub>SS</sub></b> Most negative power supply potential.	<b>C<sub>IN</sub></b> Digital input capacitance.
<b>GND</b> Ground (0 V) reference.	<b>t<sub>ON</sub> (EN)</b> Delay time between the 50% and 90% points of the digital input and switch on condition.
<b>R<sub>ON</sub></b> Ohmic resistance between D and S.	<b>t<sub>OFF</sub> (EN)</b> Delay time between the 50% and 90% points of the digital input and switch off condition.
<b>R<sub>ON</sub> Drift</b> Percentage change in R <sub>ON</sub> when temperature changes by one degree Celsius.	<b>t<sub>TRANSITION</sub></b> Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.
<b>ΔR<sub>ON</sub></b> ΔR <sub>ON</sub> represents the difference between the R <sub>ON</sub> of any two channels as a percentage of the maximum R <sub>ON</sub> of those two channels.	<b>t<sub>OPEN</sub></b> Off time measured between 80% points of both switches when switching from one address state to another.
<b>I<sub>S</sub> (Off)</b> Source leakage current when the switch is off.	<b>V<sub>INL</sub></b> Maximum input voltage for Logic 0.
<b>I<sub>D</sub> (Off)</b> Drain leakage current when the switch is off.	<b>V<sub>INH</sub></b> Minimum input voltage for Logic 1.
<b>I<sub>D</sub>, I<sub>S</sub> (On)</b> Channel leakage current when the switch is on.	<b>I<sub>INL</sub> (I<sub>INH</sub>)</b> Input current of the digital input.
<b>I<sub>S</sub> (Fault—Power Supplies On)</b> Source leakage current when exposed to an overvoltage condition.	<b>Off Isolation</b> A measure of unwanted signal coupling through an off channel.
<b>I<sub>D</sub> (Fault—Power Supplies On)</b> Drain leakage current when exposed to an overvoltage condition.	<b>Charge Injection</b> A measure of the glitch impulse transferred from the digital input to the analog output during switching.
<b>I<sub>S</sub> (Fault—Power Supplies Off)</b> Source leakage current with power supplies off.	<b>I<sub>DD</sub></b> Positive supply current.
<b>V<sub>D</sub> (V<sub>S</sub>)</b> Analog Voltage on Terminals D, S.	<b>I<sub>SS</sub></b> Negative supply current.
<b>C<sub>S</sub> (Off)</b> Channel input capacitance for off condition.	

## THEORY OF OPERATION

The **ADG508F/ADG509F** multiplexers are capable of withstanding overvoltages from  $-40\text{ V}$  to  $+55\text{ V}$ , irrespective of whether the power supplies are present or not. Each channel of the multiplexer consists of an n-channel MOSFET, a p-channel MOSFET, and an n-channel MOSFET, connected in series. When the analog input exceeds the power supplies, one of the MOSFETs will saturate limiting the current. The current during a fault condition is determined by the load on the output. Figure 17 illustrates the channel architecture that enables these multiplexers to withstand continuous overvoltages.

When an analog input of  $V_{SS} + 2.2\text{ V}$  to  $V_{DD} - 2.2\text{ V}$  (output loaded,  $1\text{ mA}$ ) is applied to the **ADG508F/ADG509F**, the multiplexer behaves as a standard multiplexer, with specifications similar to a standard multiplexer, for example, the on-resistance is  $390\ \Omega$  maximum. However, when an overvoltage is applied to the device, one of the three MOSFETs saturate.

Figure 17 to Figure 20 show the conditions of the three MOSFETs for the various overvoltage situations. When the analog input applied to an on channel approaches the positive power supply line, the n-channel MOSFET saturates because the voltage on the analog input exceeds the difference between  $V_{DD}$  and the n-channel threshold voltage ( $V_{TN}$ ). When a voltage more negative than  $V_{SS}$  is applied to the multiplexer, the p-channel MOSFET will saturate because the analog input is more negative than the difference between  $V_{SS}$  and the p-channel threshold voltage ( $V_{TP}$ ). Because  $V_{TN}$  is nominally  $1.4\text{ V}$  and  $V_{TP} - 1.4\text{ V}$ , the analog input range to the multiplexer is limited to  $V_{SS} + 1.4\text{ V}$  to  $V_{DD} - 1.4\text{ V}$  (output open circuit) when a  $\pm 15\text{ V}$  power supply is used.

When the power supplies are present but the channel is off, again either the p-channel MOSFET or one of the n-channel MOSFETs will remain off when an overvoltage occurs.

Finally, when the power supplies are off, the gate of each MOSFET will be at ground. A negative overvoltage switches on the first n-channel MOSFET but the bias produced by the overvoltage causes the p-channel MOSFET to remain turned off. With a positive overvoltage, the first MOSFET in the series will remain off because the gate to source voltage applied to this MOSFET is negative.

During fault conditions (power supplies off), the leakage current into and out of the **ADG508F/ADG509F** is limited to a few microamps. This protects the multiplexer and succeeding circuitry from over stresses as well as protecting the signal sources which drive the multiplexer. Also, the other channels of the multiplexer will be undisturbed by the overvoltage and will continue to operate normally.

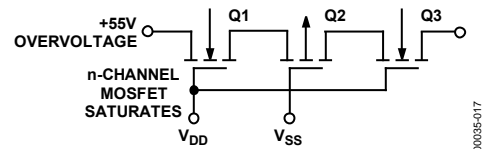


Figure 17. +55 V Overvoltage Input to the On Channel

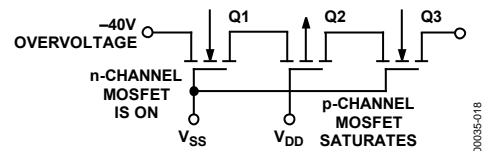


Figure 18.  $-40\text{ V}$  Overvoltage on an Off Channel with Multiplexer Power On



Figure 19. +55 V Overvoltage with Power Off



Figure 20.  $-40\text{ V}$  Overvoltage with Power Off

## TEST CIRCUITS

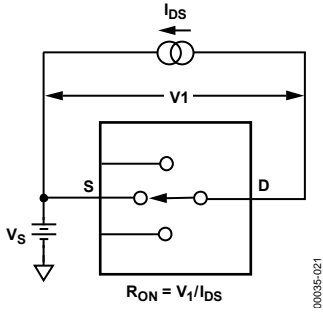


Figure 21. On Resistance

00035-021

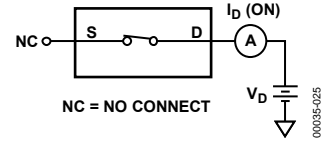


Figure 24.  $I_D$  (On)

00035-025

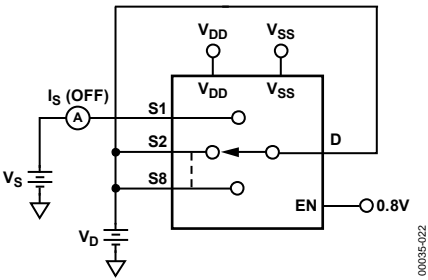


Figure 22.  $I_S$  (Off)

00035-022

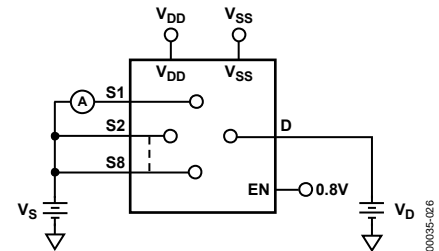


Figure 25. Input Leakage Current (with Overvoltage)

00035-026

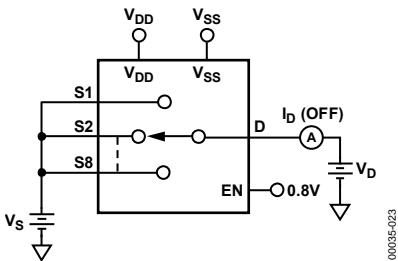


Figure 23.  $I_D$  (Off)

00035-023

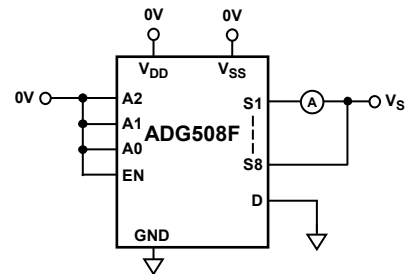


Figure 26. Input Leakage Current (with Power Supplies Off)

00035-027

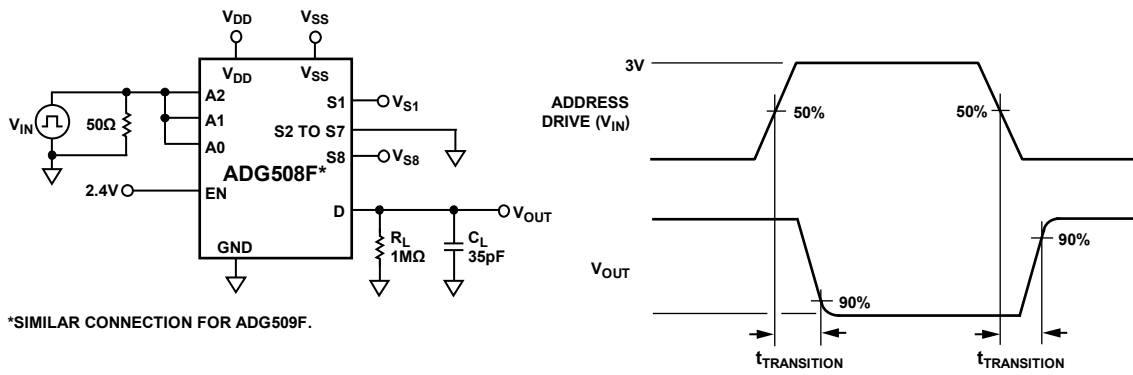


Figure 27. Switching Time of Multiplexer,  $t_{\text{TRANSITION}}$

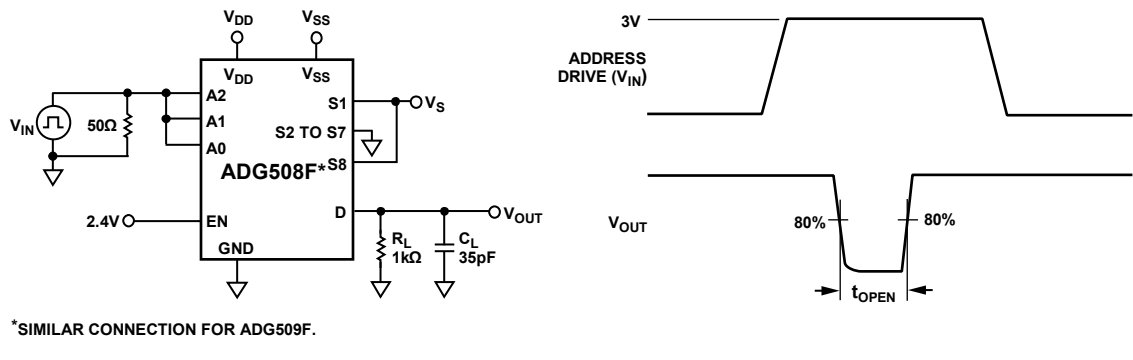


Figure 28. Break-Before-Make Delay,  $t_{\text{OPEN}}$

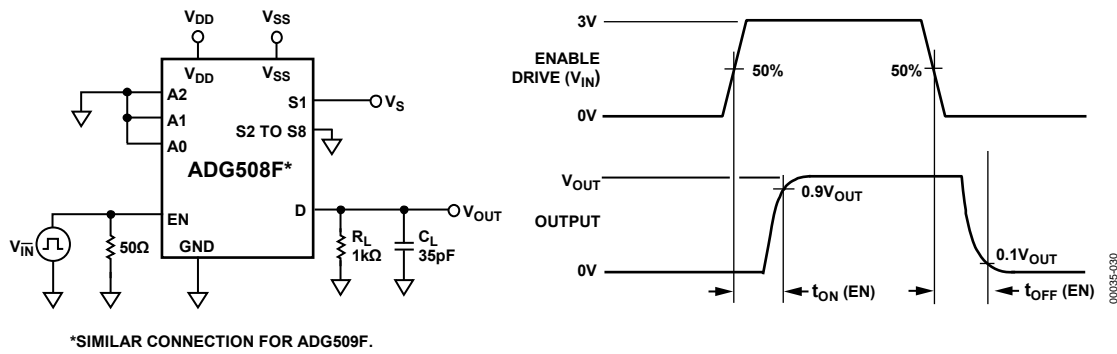


Figure 29. Enable Delay,  $t_{\text{ON}}(\text{EN})$ ,  $t_{\text{OFF}}(\text{EN})$

# ADG508F/ADG509F

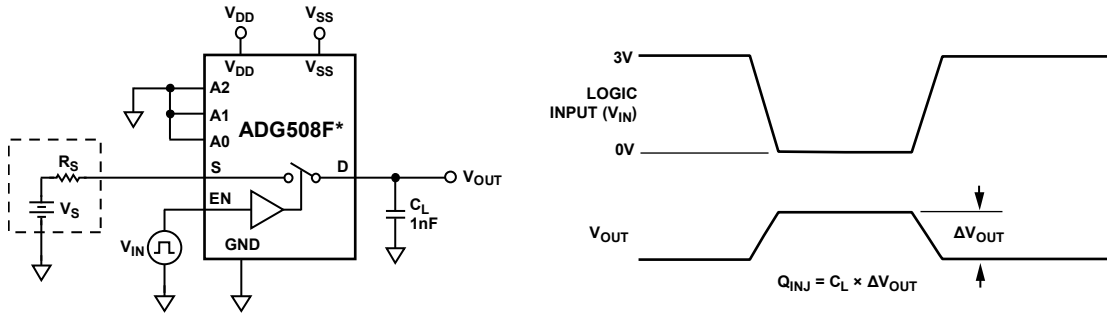


Figure 30. Charge Injection

00035-033

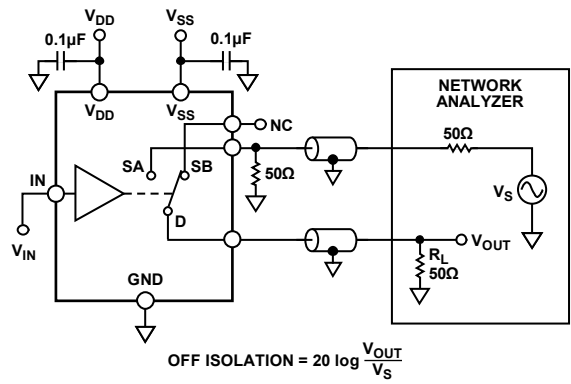
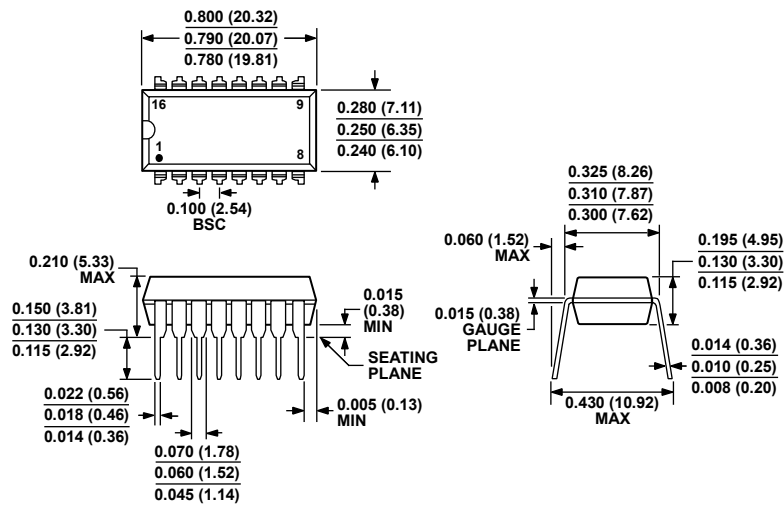


Figure 31. Off Isolation

00035-034

OUTLINE DIMENSIONS

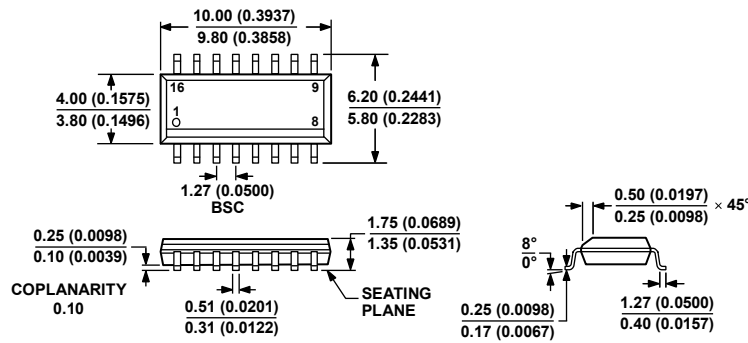


COMPLIANT TO JEDEC STANDARDS MS-001-AB  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.  
 CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 32. 16-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-16)

Dimensions shown in inches and (millimeters)

073106-B



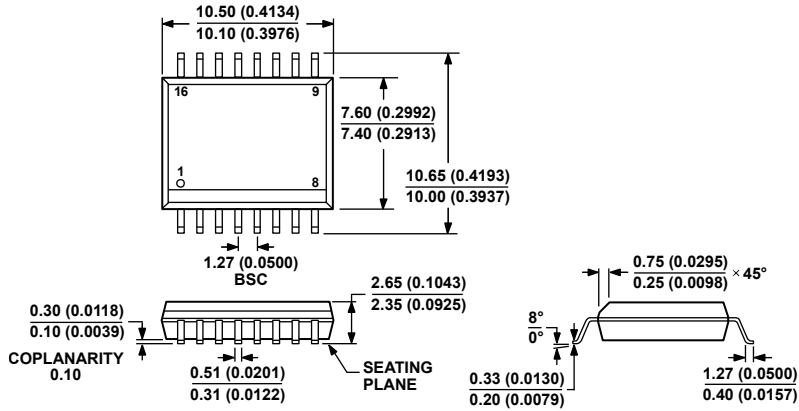
COMPLIANT TO JEDEC STANDARDS MS-012-AC  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 33. 16-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-16)

Dimensions shown in millimeters and (inches)

065636-A

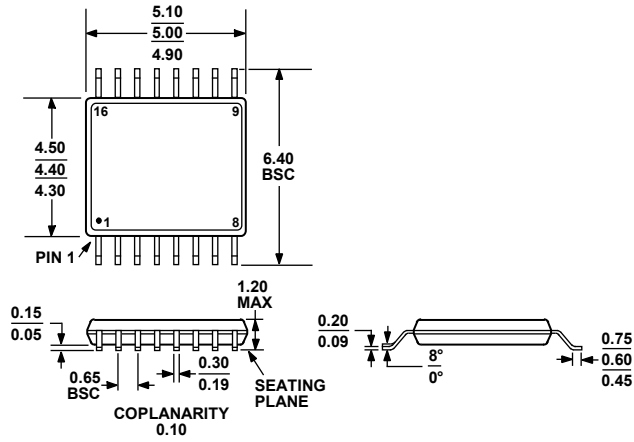
# ADG508F/ADG509F



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 34. 16-Lead Standard Small Outline Package [SOIC\_W] Wide Body  
 (RW-16)  
 Dimensions shown in millimeters and (inches)

03-27-2007-B



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP]  
 (RU-16)  
 Dimensions shown in millimeters



**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG508FBNZ	–40°C to +85°C	16-Lead PDIP	N-16
ADG508FBRN	–40°C to +85°C	16-Lead SOIC_N	R-16
ADG508FBRNZ	–40°C to +85°C	16-Lead SOIC_N	R-16
ADG508FBRNZ-REEL7	–40°C to +85°C	16-Lead SOIC_N	R-16
ADG508FBRWZ	–40°C to +85°C	16-Lead SOIC_W	RW-16
ADG508FBRWZ-REEL	–40°C to +85°C	16-Lead SOIC_W	RW-16
ADG508FBRUZ	–40°C to +85°C	16-Lead TSSOP	RU-16
ADG508FBRUZ-REEL7	–40°C to +85°C	16-Lead TSSOP	RU-16
ADG509FBNZ	–40°C to +85°C	16-Lead PDIP	N-16
ADG509FBRN	–40°C to +85°C	16-Lead SOIC_N	R-16
ADG509FBRNZ	–40°C to +85°C	16-Lead SOIC_N	R-16
ADG509FBRNZ-REEL7	–40°C to +85°C	16-Lead SOIC_N	R-16
ADG509FBRWZ	–40°C to +85°C	16-Lead SOIC_W	RW-16
ADG509FBRWZ-REEL	–40°C to +85°C	16-Lead SOIC_W	RW-16
ADG509FBRUZ	–40°C to +85°C	16-Lead TSSOP	RU-16
ADG509FBRUZ-REEL7	–40°C to +85°C	16-Lead TSSOP	RU-16

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

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