November 1999
Revised March 2005

USB1T11A
Universal Serial Bus Transceiver

General Description

The USB1T11A is a one chip generic USB transceiver. It is designed to allow 5.0V or 3.3V programmable and standard logic to interface with the physical layer of the Universal Serial Bus. It is capable of transmitting and receiving serial data at both full speed (12Mbit/s) and low speed (1.5Mbit/s) data rates.

The input and output signals of the USB1T11A conform with the "Serial Interface Engine". Implementation of the Serial Interface Engine along with the USB1T11A allows the designer to make USB compatible devices with off-the-shelf logic and easily modify and update the application.

Features

- Complies with Universal Serial Bus specification 1.1
- Utilizes digital inputs and outputs to transmit and receive USB cable data
- Supports 12Mbit/s "Full Speed" and 1.5Mbit/s "Low Speed" serial data transmission
- Compatible with the VHDL "Serial Interface Engine" from USB Implementers' Forum
- Supports single-ended data interface
- Single 3.3V supply
- ESD Performance: Human Body Model
  - > 9.5 kV on D–, D+ pins only
  - > 4 kV on all other pins
- 16-lead Pb-Free MLP package saves space

Ordering Code:

Order Number	Package Number	Package Description
USB1T11AM (Note 1)	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
USB1T11AM_NL (Note 2)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
USB1T11ABQX	MLP16C	Pb-Free 16-Terminal Molded Leadless Package (MLP), JEDEC MO-220, 3mm square
USB1T11AMTC (Note 1)	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
USB1T11AMTC_NL (Note 2)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
USB1T11AMTCX_NL (Note 2)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

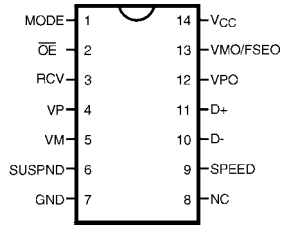
Pb-Free package per JEDEC J-STD-020B.

Note 1: Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

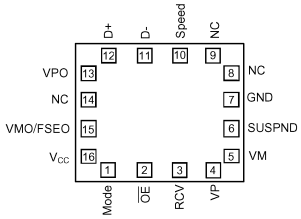
Note 2: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Please use order number as indicated.

Connection Diagrams

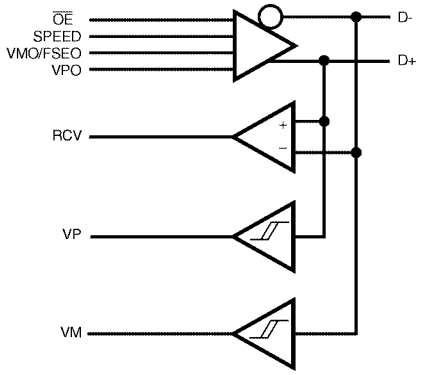
Pin Assignments for SOIC and TSSOP



Pin Assignments for MLP



Logic Diagram



Pin Descriptions

Pin Name	I/O	Description
RCV	O	Receive data. CMOS level output for USB differential input
$\overline{OE}$	I	Output Enable. Active LOW, enables the transceiver to transmit data on the bus. When not active the transceiver is in receive mode.
MODE	I	Mode. When left unconnected, a weak pull-up transistor pulls it to V_{CC} and in this GND, the VMO/FSEO pin takes the function of FSEO (Force SEO).
V_{PO}, V_{MO}/F_{SEO}	I	Inputs to differential driver. (Outputs from SIE).

MODE	VPO	VMO/FSEO	RESULT
0	0	0	Logic “0”
	0	1	$\overline{SE0}$
	1	0	Logic “1”
	1	1	$\overline{SEO}$
1	0	0	$\overline{SE0}$
	0	1	Logic “0”
	1	0	Logic “1”
	1	1	Illegal code

V_P, V_M	O	Gated version of D– and D+. Outputs are logic “0” and logic “1”. Used to detect single ended zero ($\overline{SE0}$), error conditions, and interconnect speed. (Input to SIE).

VP	VM	RESULT
0	0	$\overline{SE0}$
0	1	Low Speed
1	0	Full Speed
1	1	Error

D+, D–	AI/O	Data+, Data–. Differential data bus conforming to the Universal Serial Bus standard.
SUSPND	I	Suspend. Enables a low power state while the USB bus is inactive. While the suspend pin is active it will drive the RCV pin to a logic “0” state. Both D+ and D– are 3-STATE.
SPEED	I	Edge rate control. Logic “1” operates at edge rates for “full speed”. Logic “0” operates edge rates for “low speed”.
V_{CC}		3.0V to 3.6V power supply
GND		Ground reference

Functional Truth Table

Input					I/O		Outputs			
Mode	**VPO**	**VMO/FSEO**	**$\overline{OE}$**	**SUSPND**	**D_+**	**D_-**	**RCV**	**V_P**	**V_M**	**Result**
0	0	0	0	0	0	1	0	0	1	Logic 0
0	0	1	0	0	0	0	U	0	0	$\overline{SEO}$
0	1	0	0	0	1	0	1	1	0	Logic 1
0	1	1	0	0	0	0	U	0	0	$\overline{SEO}$
1	0	0	0	0	0	0	U	0	0	$\overline{SEO}$
1	0	1	0	0	0	1	0	0	1	Logic 0
1	1	0	0	0	1	0	1	1	0	Logic 1
1	1	1	0	0	1	1	U	U	U	Illegal Code
X	X	X	1	0	Z	Z	U	U	U	D_+/D_- Hi-Z
X	X	X	1	1	Z	Z	U	U	U	D_+/D_- Hi-Z

X = Don't Care
Z = 3-STATE
U = Undefined State

Absolute Maximum Ratings(Note 3)

DC Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I < 0$	−50 mA
Input Voltage (V_I)	
(Note 4)	−0.5V to +5.5V
Input Voltage ($V_{I/O}$)	−0.5V to V_{CC} + 0.5V
Output Diode Current (I_{OK})	
$V_O > V_{CC}$ or $V_O < 0$	±50 mA
Output Voltage (V_O)	
(Note 4)	−0.5V to V_{CC} + 0.5V
Output Source or Sink Current (I_O)	
VP.VM, RCV pins	
V_O = 0 to V_{CC}	±15 mA
Output Source or Sink Current (I_O)	
D+/D− pins	
V_O = 0 to V_{CC}	±50 mA
V_{CC} or GND Current (I_{CC}, I_{GND})	±100 mA
Storage Temperature (T_{STO})	−60°C to + 150°C

Recommended Operating Conditions

Supply Voltage V_{CC}	3.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Input Range for AI/O ($V_{AI/O}$)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Ambient Temperature	
in free air (T_{amb})	−40°C to +85°C

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristic tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC Electrical Characteristics (Digital Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted). V_{CC} = 3.0V to 3.6V

Symbol	Parameter	Test Conditions	Limits			Unit
			Temp = −40°C to +85°C			
			Min	Typ	Max	
	INPUT LEVELS:					
V_{IL}	LOW Level Input Voltage				0.8	V
V_{IH}	HIGH Level Input Voltage		2.0			V
	OUTPUT LEVELS:					
V_{OL}	LOW Level Output Voltage	I_{OL} = 4 mA			0.4	V
		I_{OL} = 20 μA			0.1	
V_{OH}	HIGH Level Output Voltage	I_{OH} = 4 mA	2.4			V
		I_{OH} = 20 μA	V_{CC} − 0.1			
	LEAKAGE CURRENT:					
I_L	Input Leakage Current	V_{CC} = 3.0 to 3.6			±5	μA
I_{CCFS}	Supply Current (Full Speed)	V_{CC} = 3.0 to 3.6			5	mA
I_{CCLS}	Supply Current (Low Speed)	V_{CC} = 3.0 to 3.6			5	mA
I_{CCQ}	Quiescent Current	V_{CC} = 3.0 to 3.6 V_{IN} = V_{CC} or GND			5	mA
I_{CCS}	Supply Current in Suspend	V_{CC} = 3.0 to 3.6; Mode = V_{CC}			10	μA

DC Electrical Characteristics (D+/D− Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted). V_{CC} = 3.0V to 3.6V

Symbol	Parameter	Test Conditions	Limits			Units
			Temp = −40°C to +85°C			
			Min	Typ	Max	
	INPUT LEVELS:					
V_{DI}	Differential Input Sensitivity	|(D+) − (D−)|	0.2			V
V_{CM}	Differential Common Mode Range	Includes V_{DI} Range	0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8		2.0	V
	OUTPUT LEVELS:					
V_{OL}	Static Output LOW Voltage	R_L of 1.5 kΩ to 3.6V			0.3	V
V_{OH}	Static Output HIGH Voltage	R_L of 15 kΩ to GND	2.8		3.6	V
V_{CR}	Differential Crossover		1.3		2.0	V
	LEAKAGE CURRENT:					
I_{OZ}	High Z State Data Line Leakage Current	$0V < V_{IN} < 3.3V$			±5	μA
	CAPACITANCE:					
C_{IN}(Note 6)	Transceiver Capacitance	Pin to GND			10	pF
	Capacitance Match				10	%
	OUTPUT RESISTANCE:					
Z_{DRV} (Note 5)	Driver Output Resistance	Steady State Drive	4		20	Ω
	Resistance Match				10	%

Note 5: Excludes external resistor. In order to comply with USB Specification 1.1, external series resistors of 24Ω ± 1% each on D+ and D− are recommended. This specification is guaranteed by design and statistical process distribution.

Note 6: This specification is guaranteed by design and statistical process distribution.

AC Electrical Characteristics (D+/D− Pins, Full Speed)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted). V_{CC} = 3.0V to 3.6V
C_L = 50 pF; R_L = 1.5 kΩ on D+ to V_{CC}

Symbol	Parameter	Test Condition	Limits			Units
			Temp = −40°C to +85°C			
			Min	Typ	Max	
	DRIVER CHARACTERISTICS:					
		10% and 90%				ns
t_R	Rise Time	Figure 1	4		20	
t_F	Fall Time	Figure 1	4		20	
t_{RFM}	Rise/Fall Time Matching	(t_r/t_f)	90		110	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
	DRIVER TIMINGS:					
t_{PLH}	Driver Propagation Delay	Figure 2			18	ns
t_{PLH}	(VPO, VMO/FSEO to D+/D−)	Figure 2			18	ns
t_{PHZ}	Driver Disable Delay	Figure 4			13	ns
t_{PLZ}	($\overline{OE}$ to D+/D−)	Figure 4			13	ns
t_{PZH}	Driver Enable Delay	Figure 4			17	ns
t_{PZL}	($\overline{OE}$ to D+/D−)	Figure 4			17	ns
	RECEIVER TIMINGS:					
t_{PLH}	Receiver Propagation Delay	Figure 3			16	ns
t_{PHL}	(D+, D− to RCV)	Figure 3			19	ns
t_{PLH}	Single-ended Receiver Delay	Figure 3			8	ns
t_{PHL}	(D+, D− to VP, VM)	Figure 3			8	ns

AC Electrical Characteristics (D+/D− Pins, Low Speed)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted). V_{CC} = 3.0V to 3.6V
C_L = 200 pF to 600 pF; R_L = 1.5kΩ on D− to V_{CC}

Symbol	Parameter	Test Conditions	Limits			Unit
			T_{amb} = −40°C to +85°C			
			Min	Typ	Max	
	DRIVER CHARACTERISTICS:					
		10% and 90%				
t_{LR}	Rise Time	Figure 1	75		300	ns
t_{LF}	Fall Time	Figure 1	75		300	
t_{RFM}	Rise/Fall Time Matching	(t_r/t_f)	80		120	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
	DRIVER TIMINGS:					
t_{PLH}	Driver Propagation Delay	Figure 2			300	ns
t_{PHL}	(VPO, VMO/FSEO to D+/D−)	Figure 2			300	ns
t_{PHZ}	Driver Disable Delay	Figure 4			13	ns
t_{PLZ}	($\overline{OE}$ to D+/D−)	Figure 4			13	ns
t_{PZH}	Driver Enable Delay	Figure 4			205	ns
t_{PZL}	($\overline{OE}$ to D+/D−)	Figure 4			205	ns
	RECEIVER TIMINGS:					
t_{PLH}	Receiver Propagation Delay	Figure 3			18	ns
t_{PHL}	(D+, D− to RCV)	Figure 3			18	ns
t_{PLH}	Single-ended Receiver Delay	Figure 3			28	ns
t_{PHL}	(D+, D− to VP, VM)	Figure 3			28	ns

AC Waveforms

V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load. (V_{CC} never goes below 3.0V)

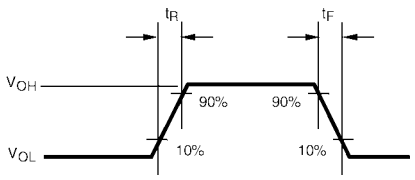


FIGURE 1. Rise and Fall Times

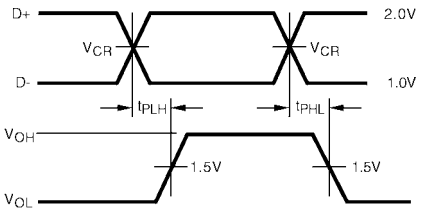


FIGURE 2. VPI, VMO/FSEO to D+/D–

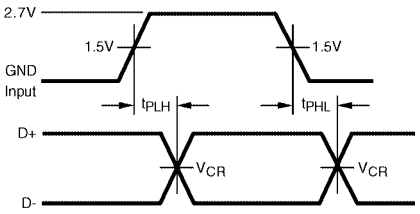


FIGURE 3. D+/D– to RCV, VP/VM

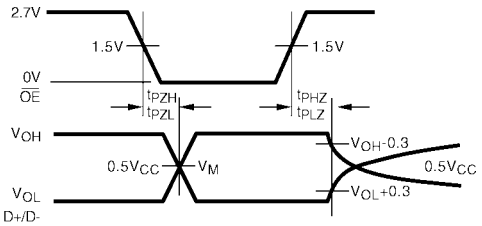
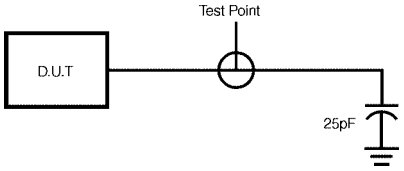
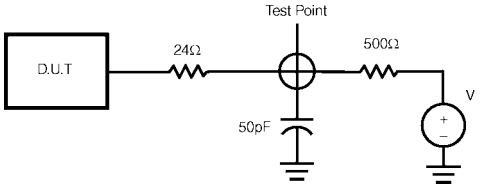


FIGURE 4. $\overline{OE}$ to D+/D–

Test Circuits and Waveforms



Load for VM/VP and RCV

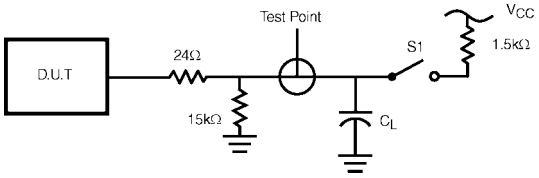


Load for Enable and Disable Times

Note:

V = 0 for t_{PZH}, t_{PHZ}

V = V_{CC} for t_{PZL}, t_{PLZ}



Load for D+/D–

Test	S1
D–/LS	Close
D+/LS	Open
D–/FS	Open
D+/FS	Close

C_L = 50 pF, Full Speed

C_L = 200 pF, Low Speed (Min Timing)

C_L = 600 pF, Low Speed (Max Timing)

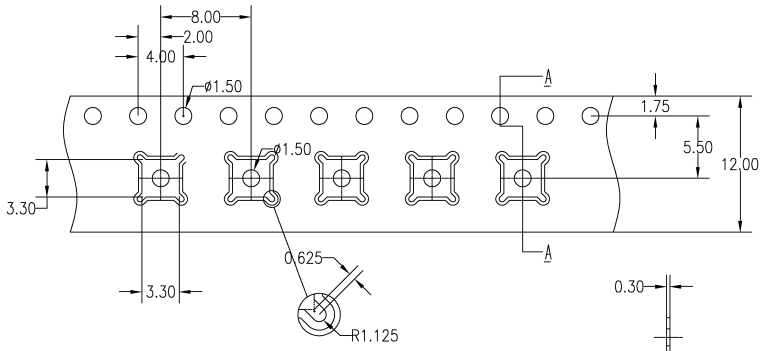
1.5 kΩ on D– (Low Speed) or D+ (Full Speed) only

Tape and Reel Specification

Tape Format for MLP

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

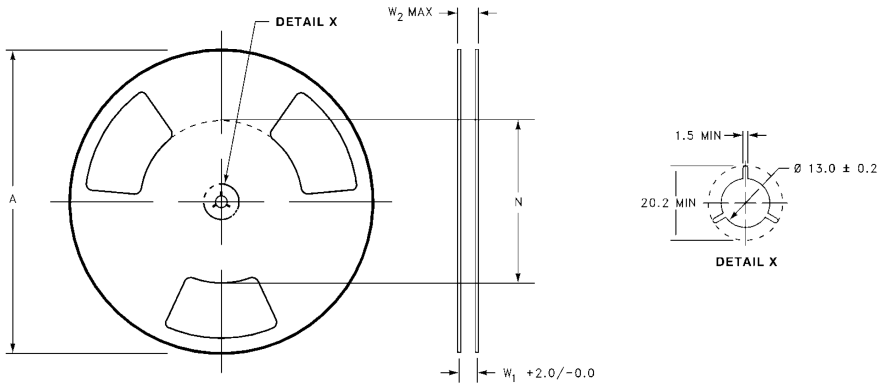
TAPE DIMENSIONS inches (millimeters)



NOTES : UNLESS OTHERWISE SPECIFIED

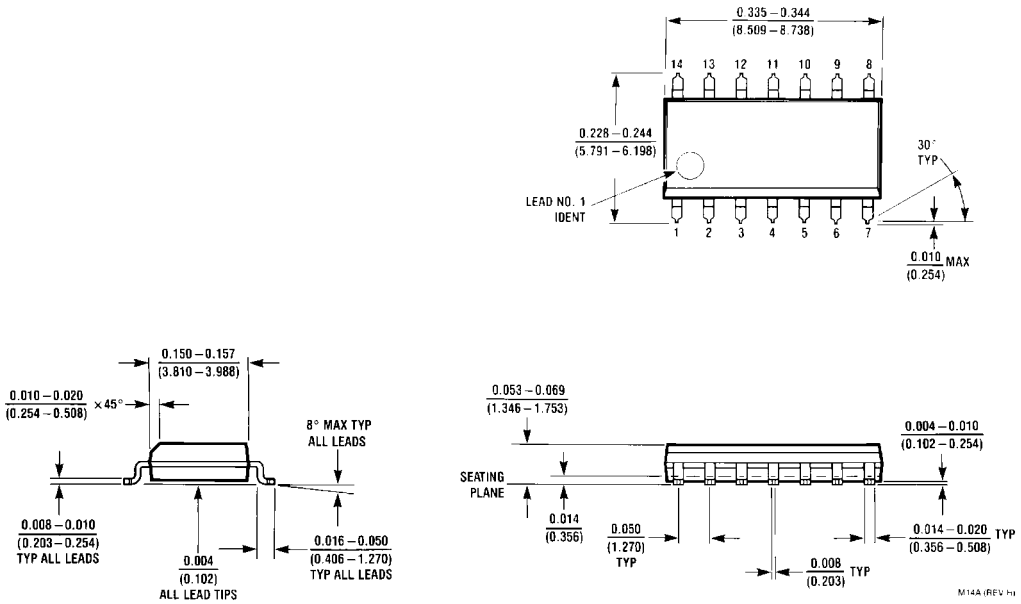
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
4. CAMBER IN COMPLIANCE WITH EIA 481
5. ADVANTEK PART DRAWING NUMBER ML0303-A

REEL DIMENSIONS inches (millimeters)



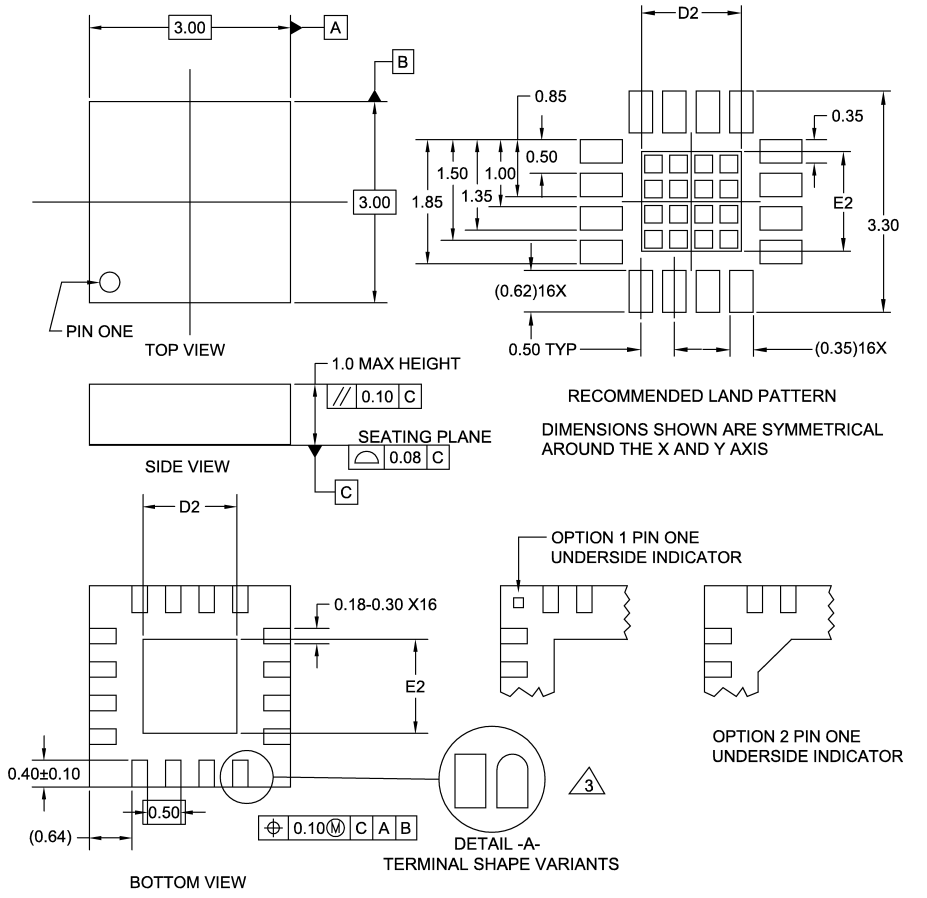
Tape Size	A (mm)	N (Typical) (mm)	W1 (mm)	W2 (Max) (mm)
12 mm	330	178	12.4	18.4

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



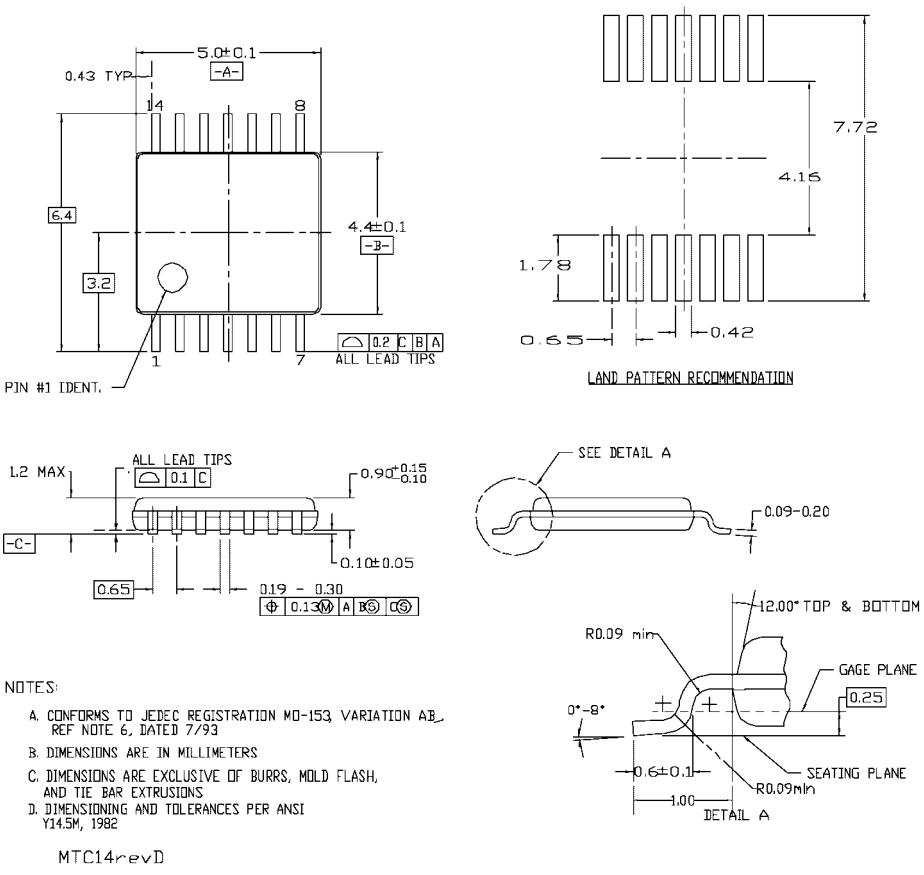
1. Package conforms to JEDEC MO-220
2. DIMENSIONS ARE IN MILLIMETERS
3. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE DETAIL A

DWG OPTION	DIM D2	DIM E2	TOLERANCE
01	1.40MM	1.40MM	+/- 0.10MM
02	1.50MM	1.50MM	+/- 0.10MM

MLP016CrevB

Pb-Free 16-Terminal Molded Leadless Package (MLP), JEDEC MO-220, 3mm square
Package Number MLP16C

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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